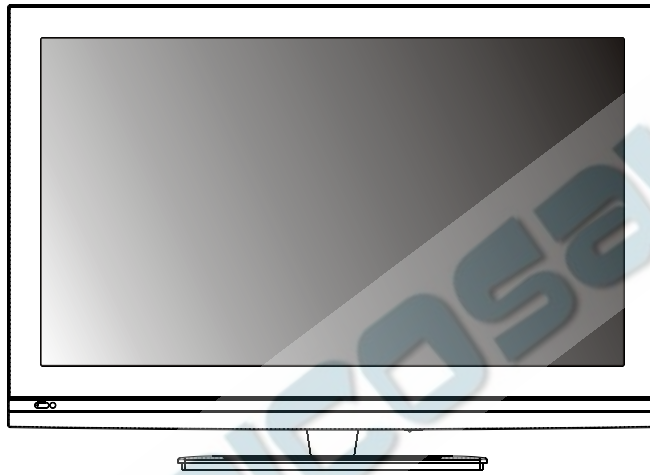


SERVICE MANUAL

8M29B CHASSIS



Design and specifications are subject to change without prior notice.
(Only Reference)

SIZE:A5

Description: SERVICE MANUAL 8M29B	
MODEL.	Brand Name: SKYWORTH
JOB NO.	
<i>Engineering Dept:</i>	
Artwork By:	Date: 2011-5-23
Checked By:	Date:
Approved By:	Date:

Content

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Technical Specification-----3-14
8M29 Block Diagram -----15
List of key parts-----16
IC BLOCK Diagram-----17-31
MAIN PCB-TOP-----32
MAIN PCB-BOT-----33
Circuit Diagrams-----34-42

Technical Specification

1.Application Area:

This product standard is used for LCD 8M29B chassis.

2.Specification:

All the standard are measured under following conditions without other specification.

- 2.1 Ambient Temperature:20+/-5°C
- 2.2 Relative Humidity:65+/-10%
- 2.3 Power Supply Voltage: Standard Input Voltage(100V~240Vac 50/60Hz)
- 2.4 Adjust after 20 minutes warm-up.

3.Test and check method:

- 3.1 Capability:According to nation test standard
- 3.2 Safety:_____ standard
EMC:_____ standard

Technical Specification

4. Safety and Regulation

No	Item	Min	Typ	Max	Unit	Remark
1.	Force Stability – Incline Plane Tip Test		10		deg	
2.	Force Stability – Level Tip Test		100		N	
3.	Isolation Gap, AC-AC/ AC-DC	3			mm	
4.	Isolation Gap	6			mm	
5.	Power Consumption, Max		105		W	For 32LED
			140		W	For 42LED
					W	
6.	Power Consumption, Stand by			1	W	
7.	Dielectric Voltage	3			kV	
8.	Isolation Resistance	4			M Ω	
9.	Leakage Current		5		mApp	
10.	Power Cord Captivity		40		N	
11.	Flammability – Back Cover		PASS			
12.	Sharp Edge		PASS			
13.	UL Compliance		NO			
14.	FCC Compliance		NO			
15.	CDRH Radiation Compliance		NO			
16.	CSA Compliance		NO			
17.	CEB Compliance		NO			
18.	CE Compliance					Base on different order
19.	CB Compliance		YES			

5. Video

No	Item	Min	Typ	Max	Unit	Remark
1.	Linearity Distortion, Vertical		1		%	
2.	Linearity Distortion, Horizontal		1		%	
3.	Trapezoidal Distortion, Vertical		1		%	
4.	Trapezoidal Distortion, Horizontal		1		%	
5.	Over Scan, Vertical	93	95	97	%	
6.	Over Scan, Horizontal	93	95	97	%	
7.	Brightness, Maximum		400		cd/m ²	FOR 32LED
			450		cd/m ²	FOR 42LED
					cd/m ²	
8.	Video Noise Limited Sensitivity(@S/N=30db) VHF			51	dBV	
9.	Video Noise Limited Sensitivity(@S/N=30db) UHF			54	dBV	

Technical Specification

10.	Selectivity -1.5M	35			dB	
11.	Selectivity +8M	40			dB	
12.	Tuning Range	-0.7			MHz	
13.	Resolution Horizontal		1366		Lines	1920 For 42LED
14.	Resolution Vertical		768		Lines	1080 For 42LED

6. Chroma

No	Item	Min	Typ	Max	Unit	Remark
1.	White Balance, X axis		280			
2.	White Balance, Y axis		290			
3.	White Balance, Color Temperature	6500	9800	12500	kdeg	12500(266, 276) 9800(280, 290) 6500(313, 329)
4.	Color Sensitivity		30		dB	
5.	Color Burst Lock-in Range	+/-300			Hz	
6.	Color Killer Sensitivity		30		dBuv	

7. Audio

No	Item	Min	Typ	Max	Unit	Remark
1.	Audio Noise Limited Sensitivity, VHF-L		25		dBuv	
2.	Audio Noise Limited Sensitivity, VHF-H		25		dBuv	
3.	Audio Noise Limited Sensitivity, UHF		28		dBuv	
4.	Buzz (S/N Ratio)		40		dB	
5.	Distortion		3		%	
6.	Audio Output, L/R, at 10% THD		8		W	
7.	Audio Output, Center		8		W	
8.	Stereo Separation		21		dB	
9.	Speaker Impedance		8		ohm	
10.	Speaker Power Rating		10	15	W	

Technical Specification

8. Power

No	Item	Min	Typ	Max	Unit	Remark
1.	DC Voltage, Audio		24		V	
2.	DC Voltage, Tuner(5)		5		V	

9. External Interface

No	Item	Min	Typ	Max	Unit	Remark
1.	Video Input Level		1		Vpp	75 OHM
2.	Video Input Frequency Response	4.5			MHz	
3.	Video Input S/N		40		dB	
4.	Audio Input Level		0.5		Vrms	
5.	Audio Input Frequency Response			15	kHz	
6.	Audio Input S/N		40		dB	
7.	Audio Input Distortion		3		%	
8.	Audio Input Dynamic Range			2	V	
9.	Video Output Level		1		Vpp	
10.	Video Output Frequency Response		4.2		MHz	
11.	Video Output S/N		50		dB	
12.	Audio Output Level		0.5		Vrms	
13.	Audio Output Frequency Response	80		12000	Hz	
14.	Audio Output S/N		40		dB	
15.	Audio Output Distortion		6		%	

Technical Specification

16.	Video Input Level, R/G/B		0.7		Vpp	
17.	Video Input Level, Component(Y, P _B , P _R)		0.7		Vpp	75 ohm
18.	RGB Input Resolution, Vertical		768		pixel	1080 For 42LED
19.	RGB Input Resolution, Horizontal		1366		pixel	1920 For 42LED
20.	RGB Input Horizontal Frequency		68		kHz	
21.	RGB Input Frame Rate		60		Hz	

10. The others

No	Item	Min	Typ	Max	Unit	Remark
1.	Search Sensitivity		40		dBuv	
2.	Clock, real time gain or loss (sec per day)		NO		sec	
3.	Soft Ware Functionality Test		YES			
4.	REMOCON Working Sensitivity, Straight		8		m	
5.	REMOCON Working Sensitivity, T/B/L/R		6		m	
6.	Closed Caption Sensitivity		46		dBuv	
7.	Teletext Sensitivity		46		dBm	
8.	Resonance of unit (Sweep freq : 50 ~ 1000)		NO			

11. Customer Menu Setup (as shipped condition)

No	Item	Specification	Remark
1.	PSM	Standard	
2.	SSM	Standard	
3.	Volume	20	
4.	Mute	Off	
5.	Input Mode	RF	
6.	Customer Menu Language	English	Base on different order
7.	AVL	Off	
8.	Sleep Timer	Off	
9.	Auto Sleep	Off	
10.	Blue Back	No	
11.	Surround	Off	
12.	Caption	Off	
13.	Noise Reducer	Middle	"Low" in some status

Technical Specification

12. Reliability

No	Item	Min	Typ	Max	Unit	Remark
1.	ESD		4		kV	IEC-1000-4-2
2.	EFT/Burst				kV	IEC-1000-4-4
3.	Surge Immunity				kV	IEC-1000-4-5
4.	Voltage Dip Test, 10ms				%	IEC-1000-4-11
5.	Voltage Dip Test, 100ms				%	IEC-1000-4-11
6.	Operation Temperature				deg	
7.	Operation Humidity				%	
8.	Storage Temperature				deg	
9.	MTBF (Confidence Level : 90 %)				hour	

Technical Specification

DTV-PRODUCTOINS SPECIFICATION

Model #	32"~46"
Country(West Eu./East Eu./Russia/AP/US/S.A./Japan/...)	Brazil & Argentina
Brand	Skyworth/ODM
Category (Monitor/TV/Combo/Portable TV...)	TV
Panel technology (LCD / PDP)	LCD/LED
Market Position (High/Mid/Access,,)	Class
Cabinet Design (Example: 01,23 series)	K06/E60
Product Nb	-
Chassis solution	MSD309
Chassis name	8M29B
Chassis PCB Standard	Skyworth RGB New Standard
Predecessor (replace)	-
MP date requested (ETD)	2011.1
MP date confirmed by supplier (ETD/ETA)	-
Status(Pre./Finish)	-
Regional requirement	
Homologation (Gostandard/CE/MPTT/CB/...)	CB
RoHS	Yes
Power supply(100-240V AC +/-10%/...)	100-240V AC (-20%,+10%)
Power consumption working / Annual	-
Power consumption standby	<1W
Power plug(VDE/UL/BS/...)	UCIEE/2pins
Picture display	
Screen size : diagonale (inch)	32",42", 46"
Aspect ratio (16/9 // 4/3 // 15/9)	16:9
1st panel supplier : panel suppliers	LG
1st panel supplier : panel reference	
Panel Display Type(MVA/PVA/IPS/...)	TFT LCD
1st panel supplier : resolution	32:1366x768、 42/46:1920x1080
Dynamic contrast ratio	>10000: 1
Video signal process	
Comb Filter (2D/3D)	3D
Noise Reduction (adaptative/3D/...)	3D
Picture improvement (LTI/CTI,BLE,WLE,...)	LTI/CTI
Color process (Gama correction/Skin correction /...)	Follow main IC

Technical Specification

Colour preset (Cool/Normal/Warm/Personal)	Medium, Cool, Warm and Personal in PC mode
Picture control (Bright/Con./Sharpness/Color/Tint/...)	Yes
Picture presets : Standard / Bright / Soft / User	Standard / Mild / Film / Dynamic / Personal
Picture freeze	Yes
Multi picture : PIP (AV)/POP (AV)	No
Dynamic Backlight Control	No
LED Backlight	Yes
Deinterlacer (No/linear/motion adaptive/motion compensative)	3D motion adaptive
Film mode / reverse 3:2/2:2 pull down	Yes / Yes
Full HD support (1080P)	Yes
Single scan / Dual scan (120HZ)	32:Single scan,42/46: Dual scan(only for LED)
Zoom type : 4/3 format	Yes
Zoom type : 14/9 Zoom	Yes
Zoom type : 16/9 Zoom	16/9 ZOOM 1
Zoom type : 16/9 Zoom up/down	16/9 ZOOM 2
Zoom type : Cinerama	Yes
Zoom type : 16/9 Format	Yes
Zoom type : Auto (by SCART Pin8 and WSS)	Yes
Picture Auto adjustment (PC mode)	Yes
3D Panel Type(PR / SG)	
3D Mode	
3D To 2D (Y/N)	
2D To 3D (Y/N)	
Left / Right Swap (For PR Panel)	
Sound	
Sound type (Mono/AV stereo/Stereo)	stereo
Music Power (Watt)/RMS Power (Watt)	2 x 8W
Tone control (Bass&Treble / Graphic Equalizer)	Bass&Treble
Special sound effect (AVL / WIDE / Pseudo /...)	AVL
Surround system (Dolby / VD / SRS / BBE / ...)	Built-in Surround
Sound control (Volume , Balance , Mute)	Volume, Balance, Mute
Sound presets (User/Speech/News/Standard)	Standard / Music / Movie / Sport / Personal
Headphone volume control (Separated / linked)	Yes(Linked)
Sound quality (High / Mid / Low)	Mid
Reception and Decoding capability	
RF range (ATV)	54MHz~864MHz
RF range (DTV)	VHF 177-213 MHZ, UHF 473-803 MHZ
Color System (PAL/SECAM/NTSC/PAL M,N)	PAL M,PAL N,NTSC M
Audio Standard (B/G/H/D/K/K'/I/L/L')	M,N
Stereo audio system (Nicam,MTS,A2,...)	BTSC,SAP
Video standard NTSC 3.58 / 4.43 (AV)/PAL 60	NTSC 3.58/4.43 , PAL

Technical Specification

DTV SD support (DVB-T/S/C , ATSC , QAM , ...)	ISDB-T
DTV HD Support	MPEG2,MPEG4,H.264
MHEG5	No
HD capability with YPbPr	Yes (720p; 1080i; 1080p@24/50/60Hz; 480i/p; 576i/p)
PC capability (up to maximum format)	Up to 1280X1024 60Hz
HDMI capability (AV/PC Format)	Up to 1080P 24/50/60HZ
Compatible video format if DVD/USB: DviX/VCD/SVCD/JPEG/AVI/MPEG2/WMV- HD/SD	JPEG/MPEG2/MPEG4/H.264/DivX (depending on license)
Compatible audio format if DVD/USB: MP3/WMA/AAC/MPEG1/...	MP3/WMA(depending on license)
Playable Discs (CD/CD-R(RW)/CD-ROM/DVD+R/+RW/-R/-RW)	No
Card reader format compatibility	No
Macrovision	Yes
PVR	Yes (FOR USB)
Network	No
User convenience	
OSD Language*	English/Spanish/Portuguese/French
OSD Positioning	No
OSD Transparency Adjust	No
OSD Timeout Adjust	No
Customer Brand name(LOGO)	Yes
IB languages	English
ATV Program Numbers (example: 99+3AV input)	99+7AV
DTV Program Numbers	600
Program edit (naming , sorting , skip , swap)	Naming / Skip / Swap
Auto Naming/Auto Sorting	No
TV Guide(DTV EPG)	EPG(next Seven-day)
Favorite program	Yes
Number of buttons on cabinet (Power; Vol+/-; Pr+/-, Menu)	Vol+/-; Pr+/-, Menu ,Source,Power(optional)
Main switch button (yes/No)	Yes
CCD (Closed Caption)/V-CHIP	Yes/No
Text Standard: (Top, FLOF,,,))	No
Teletext Level: 2.5 / 1.5	-
Pages for teletext	-
Teletext character sets ****	-
DVB-T teletext	-
Real clock	From DTV
Sleep timer	10-240 Min.
Timer	Turn On / Off, Program Switch
Parent Control -Source and Channel lock (Input code for certain channel)	Yes
Parent Control - Child lock (set the lock of the keyboard, only the RCU can control the TV)	No

Technical Specification

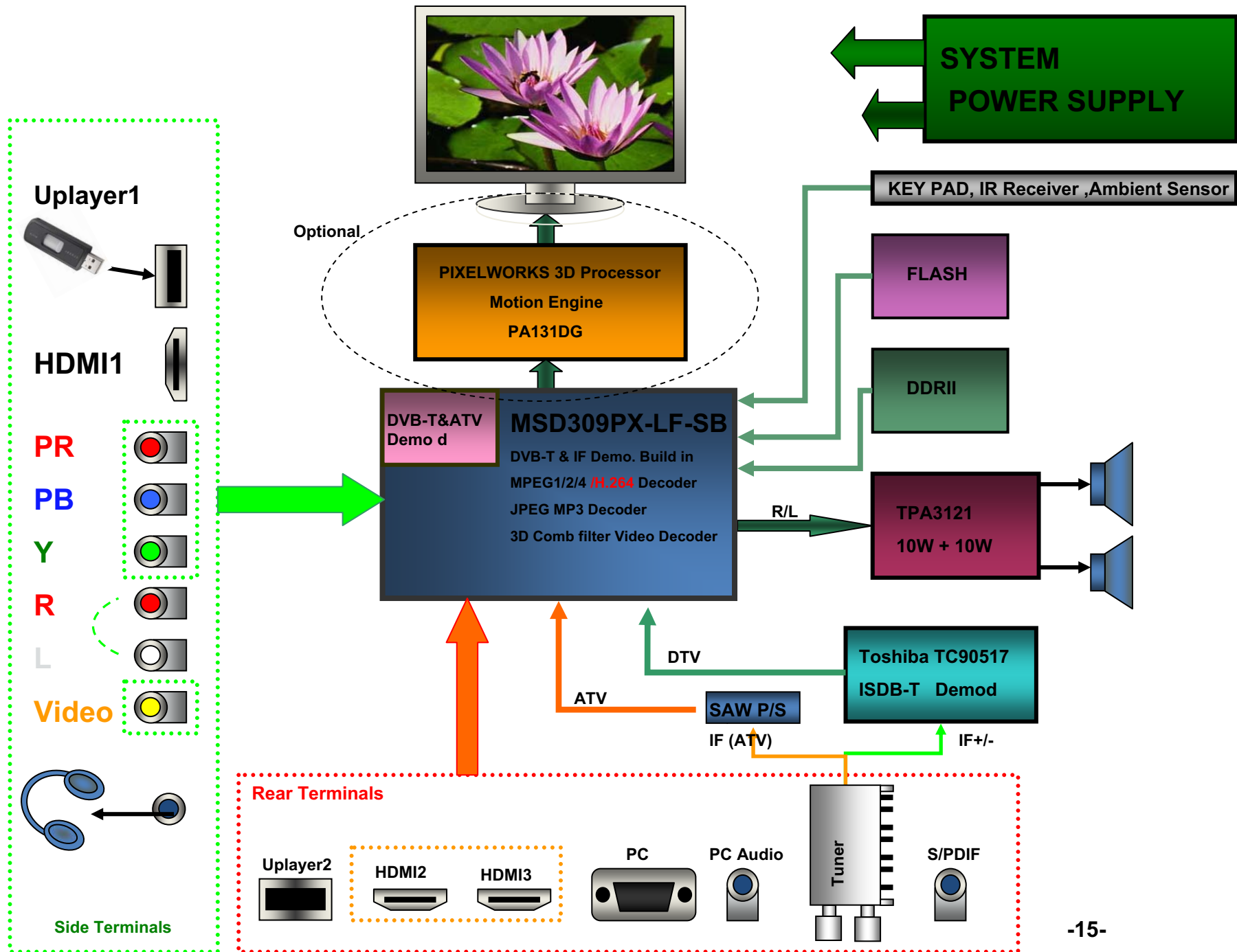
Parent Control - Kid pass (preset the ontime, channel for each day of the week)	No
Parent Control - Channel lock (For digital transmission and DVD program, to filter some programmes)	Yes
Calendar / Games	No
No program auto switch off	15 mins.
Hotel mode (Y/N)	T.B.D
DVD player (No/slot/tray)	No
Tuner FM (yes/No)	No
software download(RS232/CI/USB/OAD)	USB
Factory reset	Yes (in factory menu,reset the setting to shipment state)
Screen saver	Yes
Blue Back	No
LED indicator(Power on/Standby)	Blue / Red
Connectors -Rear	
RF Input (Antenna): Air/ Cable/ 2in1	Air+Cable
Scart : CVBS in&out / RGB / S-VIDEO	No
CINCH video in / out (AV1)	No
CINCH audio in / out (No volumpe control on Audio out/can be jack 3,5mm)	No
S-video in	No
Component Video Input (YCrCb/YPrPb)	No
Component Audio Input (YCrCb/YPrPb)	No
VGA in / Audio L/R in / Jack audio in 3.5mm	VGA + dia. 3.5mm for audio in
HDMI	2
DVI	No
Audio input for DVI	No
CINCH subwoofer out / Coaxial out (S/PDIF)	No
Headphone output connector (mm)	No
RS232 (Y/N , VGA or DB9 port ...)	No
Card Readers	No
USB slot (No/1.1/2)	1 (Software update, JPEG, MP3, WMA, RMVB, DivX) Multimedia depends on license
DVB-CI (common interface)	No
External power converter input	No
Connectors -Side	
HDMI	1
AV-IN	1
AV-OUT	No

Technical Specification

Component Video Input (YCrCb/YPrPb)	1
Component Audio Input (YCrCb/YPrPb)	1 with cable adapter
Headphone output connector (dia.mm)	1 (3.5mm)
CINCH subwoofer out / Coaxial out (S/PDIF)	S/PDIF out (optical)
USB slot (No/1.1/2)	1 (Software update, JPEG, MP3, WMA, RMVB, DivX) Multimedia depends on license
DVB-CI (common interface)	No
DLNA	No
UI/RC	
UI design (font/pixel, 2D/3D graphic engine..)	SOD Standard
RC Model	YK76B3 (Toshiba)
RC system	RGB Standard
RC # of keys	
Accessories included	
Carton (English/French/Spanish)	English
IB	English
Circuit diagram	No
Batteries	Yes
Product registration Card	Yes (English)
AC Cable Length	1.8m
Audio Cord (Jack 3.5mm)	Yes(For component audio in)
VGA Cord	No
Wallmount frame	Optional
Antenna Cable	No
6 in 1(YPbPr & CVBS) cable adapter	No
3D Glasses	No
General Data	
Size (W x H x D, with stand) in mm	-
Size (W x H x D, without stand) in mm	-
Package Size (W x H x D, without stand) in mm	-
Net Weight in kg	-
Gross Weight in Kg	-
Design / Mechanical	
Wallmount VESA compatible (standard reference)	Yes
Adaptor for VESA wallmount compatibility (accessory ref)	Yes
Desktop Stand (included/optionnal + ref/No)	included
Panel Tilt (Fowards/Backwards/Rotation)	No
Swivel function desktop stand (yes/No) + motorized?	No
Docking station (yes/No)	No
Floor Stand (included/optionnal + ref/No)	No
Glass shield (yes/No)	No
Finish on Front	-
Finish on side	-
Finish on back	-

Technical Specification

Finish on stand	-
number of colors on carton box	2
Brand logo	Customer Inlet
Other logo	No
External AC/DC Power with DC power cord (yes/No)	No
Handle (yes/No)	No
Detachable speaker (yes/No)	No
Rating Label langages	English



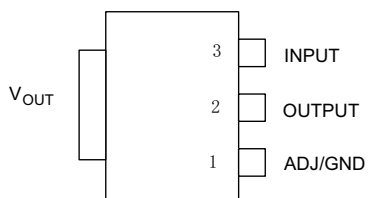
List of key parts

No.	Name	Position	Type	P/N
1	IR	U29	HS0038B4	5300-140038-0010
2	Speaker	Bass	SL-R3018H-3E	5600-106154-0060
		Treble	YDG3040-2	5600-708254-00
3	Crystal	Y2	49U3H	4900-125453-R000
		Y1	HC-49U/S	4900-124053-R000
4	Tuner	U10	VA1P1BF8405	5202-45733D-7H10
5	Saw	U30	F4401	4900-744015-0X00
6	IC	U3	MP1482DS	476A-M14820-0080
		U5	MP1482DS	476A-M14820-0080
		U50	MP1482DS	476A-M14820-0080
		U51	MP1482DS	476A-M14820-0080
		U9	W9751G6JB-25	4737-W97511-0840
		U15	W9751G6JB-25	4737-W97511-0840
		U24	EN25F32-100HIP	471R-N25321-0080
		U55	TC90517FG	4701-T90510-0640
		U37	AS1117L-3.3	47B6-A11170-03
		U38	AS1117L-3.3	47B6-A11170-03
		N1	AS1117L-3.3	47B6-A11170-03
		N2	AS1117L-1.2	47B6-A11175-0300
		U54	TPA3121D2PWPR	4722-T31210-0240
		U2	MSD309PX-LF-Z1-SB	475C-M30900-5230

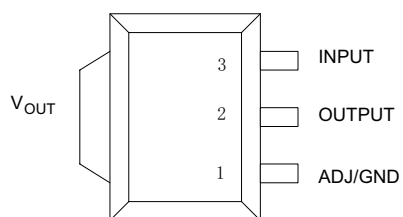
IC Block Diagram

Pin Configurations---AS1117L-3.3

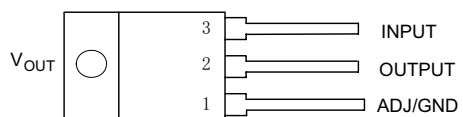
L Package
(SOT-223)



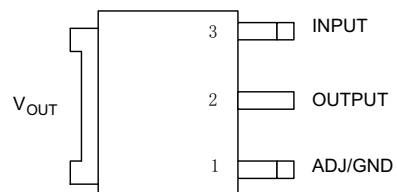
U Package
(SOT-89)



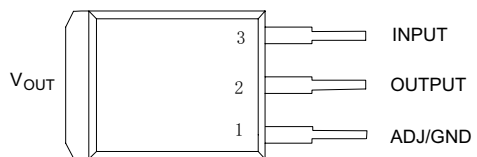
T Package
(TO-220)



R Package
(TO-252)



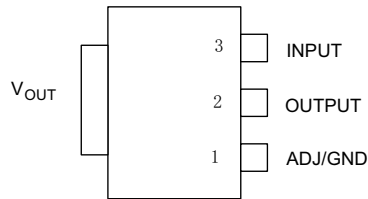
S Package
(TO-263)



IC Block Diagram

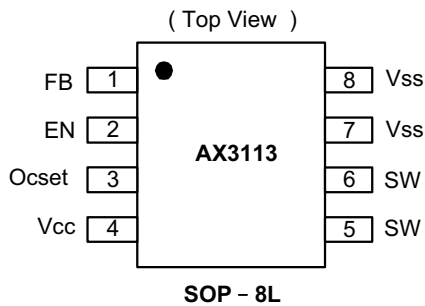
Pin Configurations---AS1117L-ADJ

L Package
(SOT-223)



❖ PIN ASSIGNMENT

The package of AX3113 is SOP-8L; the pin assignment is given by:



Name	Description
FB	Feedback pin
EN	Power-off pin H : normal operation(Step-down) L : Step-down operation stopped (All circuits deactivated)
OCSET	Add an external resistor to set max switch output current.
V_{CC}	IC power supply pin
SW	Switch pin. Connect external inductor & diode here.
V_{SS}	GND pin

IC Block Diagram

LM4558

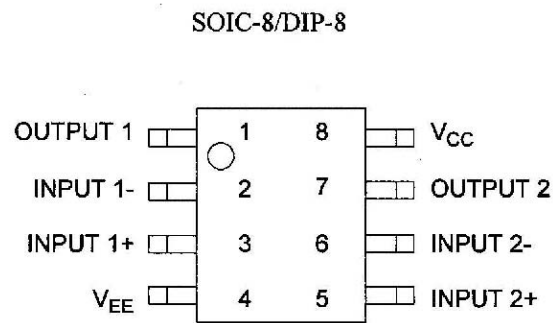
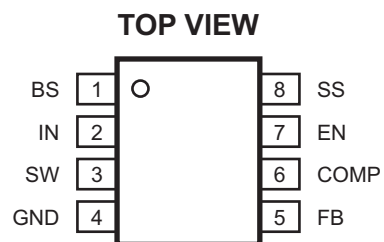


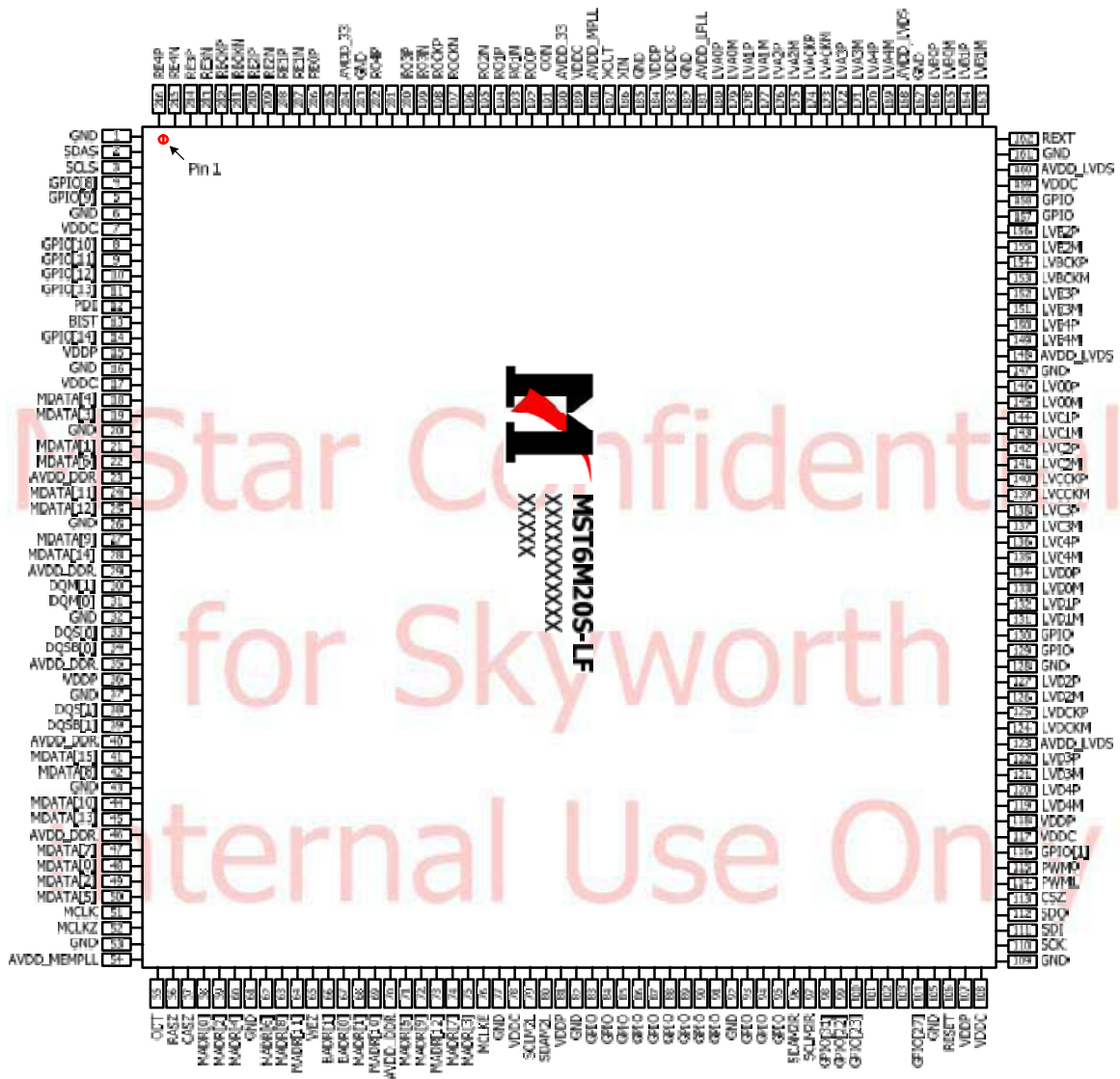
Figure 2. Pin Configuration of LM4558 (Top View)

MP1482DS



IC Block Diagram

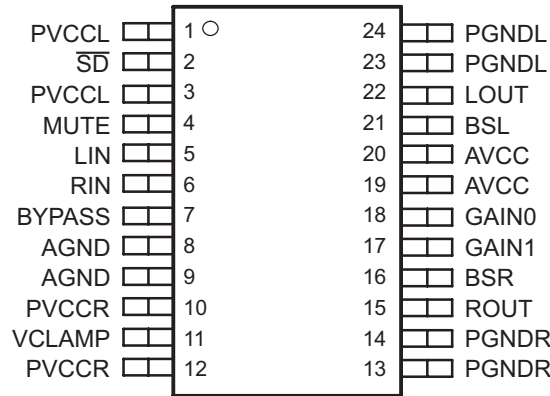
MST6M20S-LF



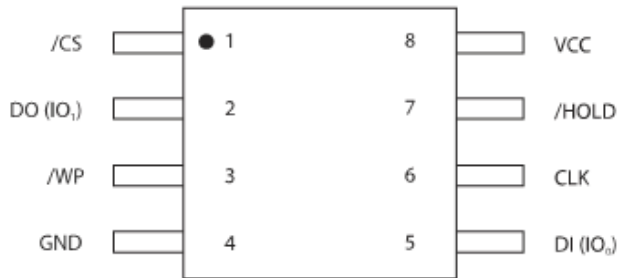
IC Block Diagram

W25X40BVSNIG

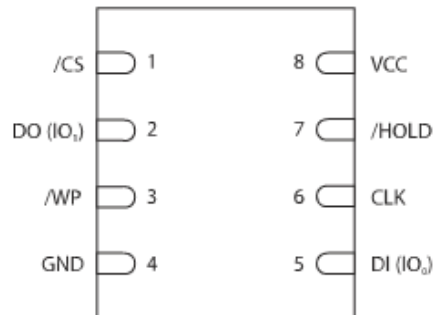
**PWP (TSSOP) PACKAGE
(TOP VIEW)**



**PIN CONFIGURATION
SOIC 150-MIL / 208-MIL**



**PAD CONFIGURATION
WSON 6X5-MM**



**PIN CONFIGURATION
PDIP 300-MIL**

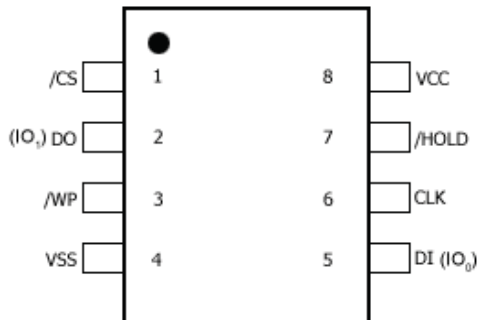
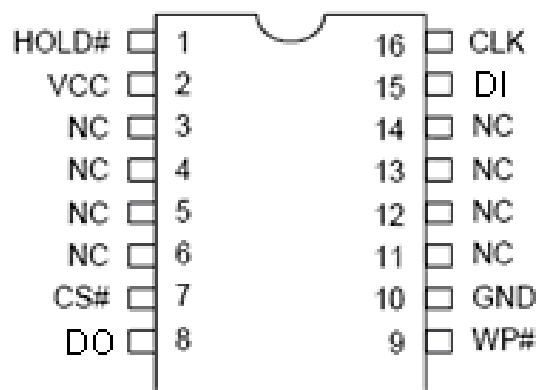
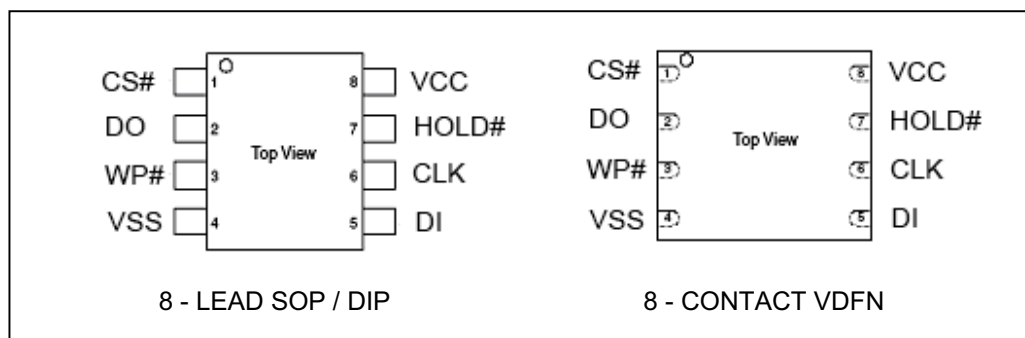




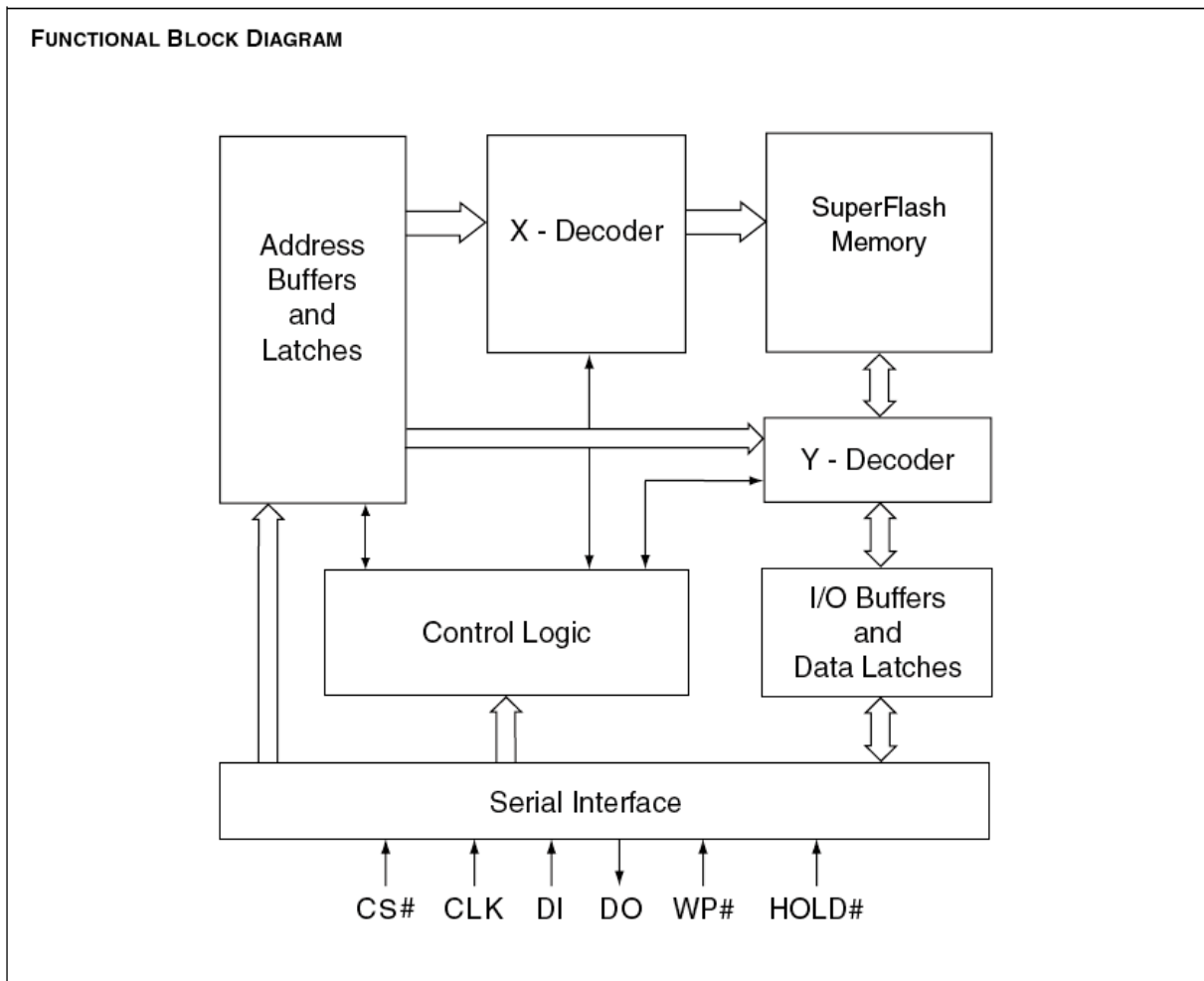
Figure.1 CONNECTION DIAGRAMS



16 - LEAD SOP



Figure 2. BLOCK DIAGRAM





SIGNAL DESCRIPTION

Serial Data Input (DI)

The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin.

Serial Data Output (DO)

The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Hold (HOLD#)

The HOLD pin allows the device to be paused while it is actively selected. When HOLD is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). The hold function can be useful when multiple devices are sharing the same SPI signals.

Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1 and BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.

Table 1. PIN Names

Symbol	Pin Name
CLK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
CS#	Chip Enable
WP#	Write Protect
HOLD#	Hold Input
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground

IC Block Diagram

TOSHIBA CONFIDENTIAL

TC90517FG Toshiba products specification [Tentative]

2. Configuration

All functions required for ISDB-T demodulation and error correction are built into the TC90517. The input signals to be supported are a low IF (intermediate frequency) signal and direct IF signal. [Baseband IQ signals can also be input.](#)

The output signal is an MPEG-2 transport stream (TS) in serial format. Note that a TS in parallel format can be output by setting registers.

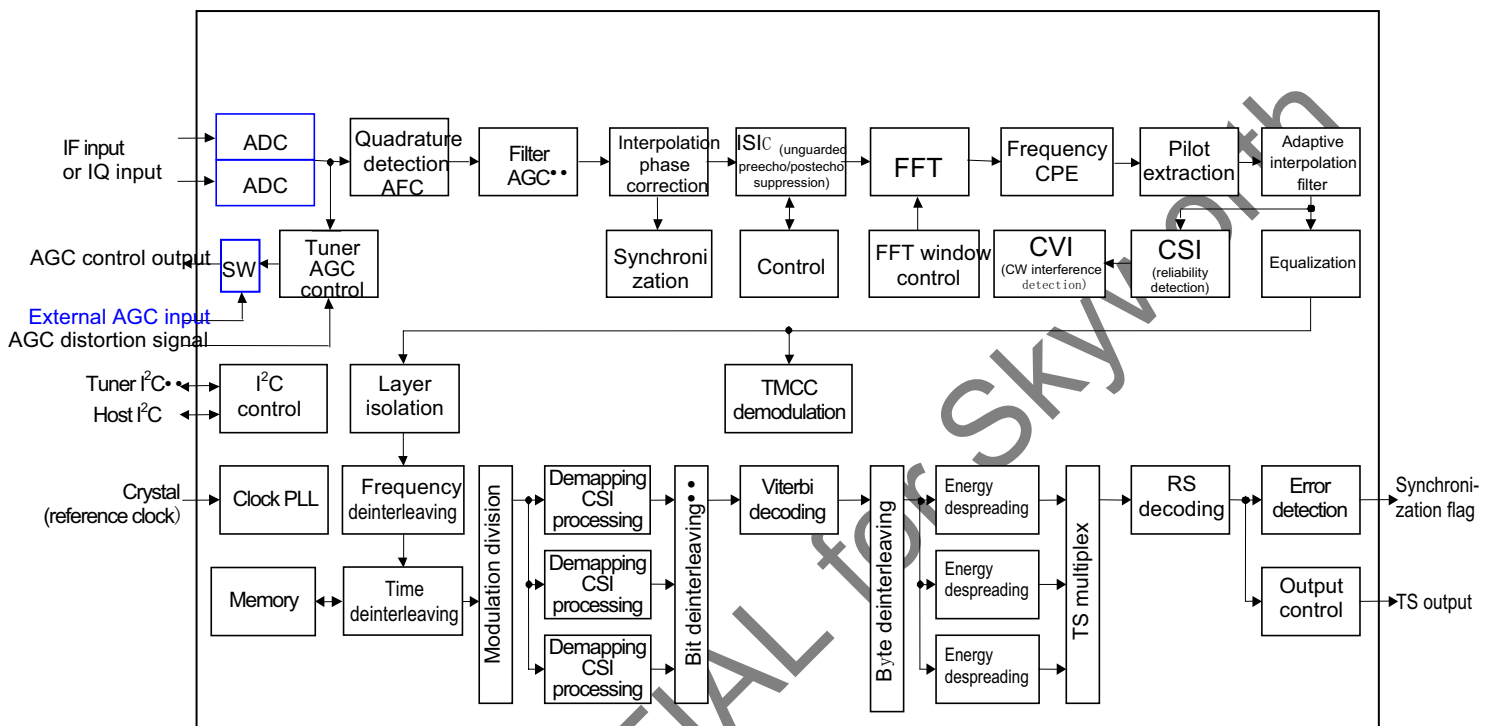


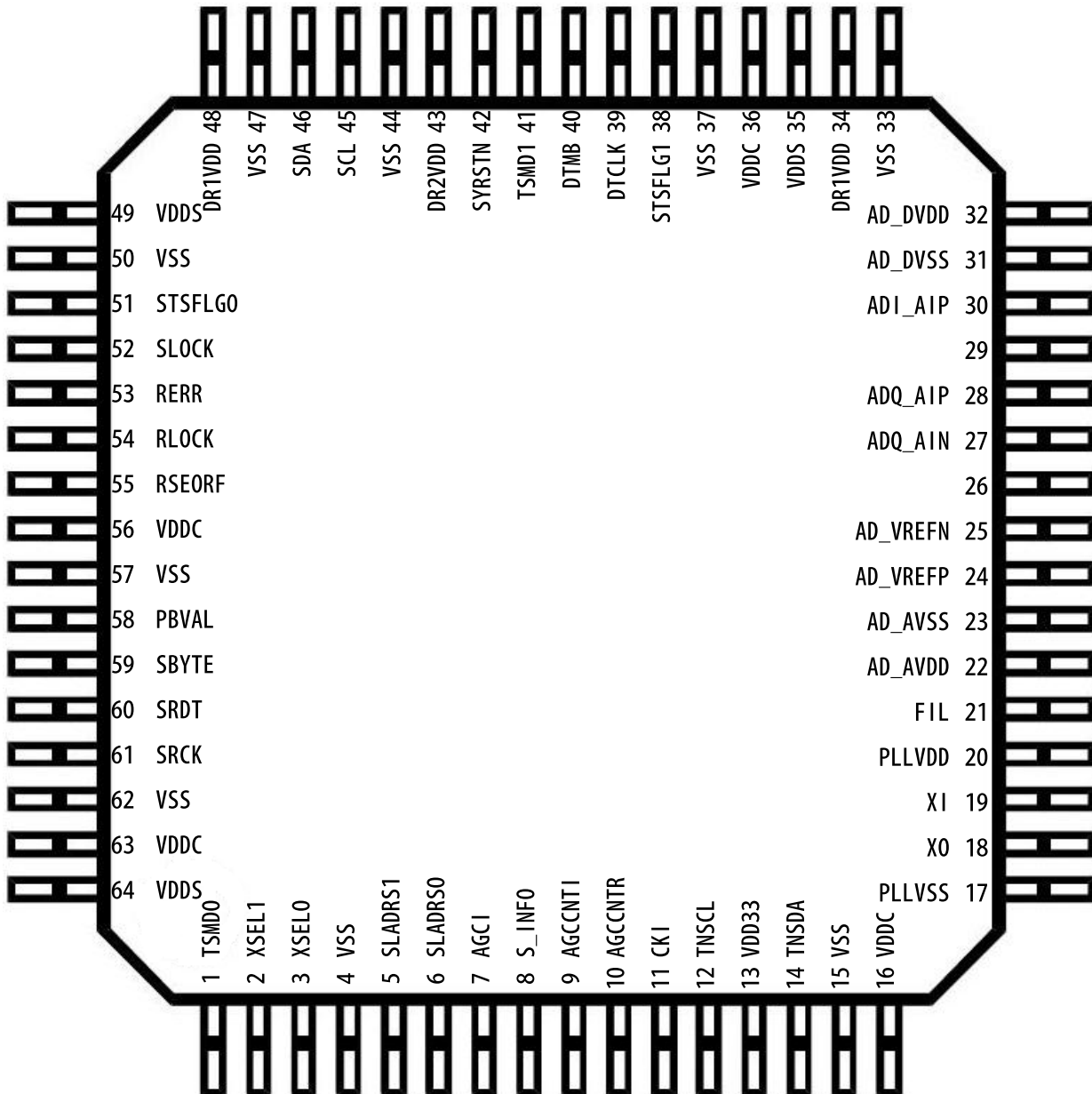
Fig. 2.1 TC90517FG Block Diagram

IC Block Diagram

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TC90517FG Toshiba products specification [Tentative]

3. Pin Assignment (Top view)



IC Block Diagram

4. Pin Functions

This specification indicates pins and their signals in upper case letters and registers and their signals in lower case letters.

Pin	Pin name	(Note4) I/O	(Note5,7) PU/PD	Function ^(Note 3)	Remarks ^(Note 2 and 6)
1	TSMD0	I	-	Shut down	0: Normal operation 1: Shut down
2	XSEL1	I	-	Crystal frequency division ratio 1	Set according to crystal frequency.
3	XSEL0	I	-	Crystal frequency division ratio 0	Set according to crystal frequency.
4	VSS	-	-	Digital GND	Connects to DGND.
5	SLADRS1	I/O	-	Slave address 1	Set according to slave address.
6	SLADRS0	I/O	-	Slave address 0	Set according to slave address.
7	AGCI	I	-	External AGC input	Connects to DGND when not used.
8	S_INFO	I	-	Pin for pre-shipment test	Connects to DGND.
9	AGCCNTI	I/O	PD	IF_AGC control output	Connects to tuner IF_AGC control input pin.
10	AGCCNTR	I/O	PD	RF_AGC control output	Connects to tuner RF_AGC control input pin. Open, fixed to L when not used.
11	CKI	I	-	Pin for pre-shipment test	Connects to DGND.
12	TNSCL	I/O	OD	I2C clock output	Connects to tuner I2C clock pin. (Pull-up performed outside IC.)
13	VDDS	-	-	I/O power supply	Connects to digital +3.3 V typ.
14	TNSDA	I/O	OD	I2C data I/O	Connects to tuner I2C data pin. (Pull-up performed outside IC.)
15	VSS	-	-	Digital GND	Connects to DGND.
16	VDDC	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
17	PLLVSS	-	-	Clock PLL GND	Connects to AGND.
18	XO	O	-	Crystal output	Connects to crystal. ixosl="1" and open when an external reference clock is input.
19	XI	I	-	Crystal or reference clock input	Connects to crystal. The amplitude (p-p) is 0.5 V to PLLVDD when an external reference clock is input.
20	PLLVDD	-	-	Clock PLL power supply	Connects to analog +2.5 V typ.
21	FIL	O	-	PLL filter output	Connects to AGND via 1500 pF.
22	AD_AVDD	-	-	ADC analog power supply	Connects to analog +2.5 V typ.
23	AD_AVSS	-	-	ADC analog GND	Connects to AGND.
24	AD_VREFP	-	-	ADC reference voltage output	+1.75 V typ. Connects to AGND via PC.
25	AD_VREFN	-	-	ADC reference voltage output	+0.75 V typ. Connects to AGND via PC.
26	AD_VREF	-	-	ADC reference voltage output	+1.25 V typ. Connects to AGND via PC.
27	ADQ_AIN	I	-	Q signal (differential negative side) input	Single-ended IF: Connects to AGND via PC. Differential IF: Connects to AGND via PC. Single-ended IQ: Connects to AGND via PC. Differential IQ: Connects to tuner Q (-) output after the DC component was cut.
28	ADQ_AIP	I	-	Q signal (differential positive side) input	Single-ended IF: Connects to AGND via PC. Differential IF: Connects to AGND via PC. Single-ended IQ: Connects to tuner Q output after the DC component was cut. Differential IQ: Connects to tuner Q (+) output after the DC component was cut.
29	ADI_AIN	I	-	IF signal (differential negative side) input or I signal (differential negative side) input	Single-ended IF: Connects to AGND via PC. Differential IF: Connects to tuner IF (-) output after the DC component was cut. Single-ended IQ: Connects to AGND via PC. Differential IQ: Connects to tuner I (-) output after the DC component was cut.
30	ADI_AIP	I	-	IF signal (differential positive side) input or I signal (differential positive side) input	Single-ended IF: Connects to tuner IF output after the DC component was cut. Differential IF: Connects to tuner IF (+) output after the DC component was cut. Single-ended IQ: Connects to tuner I output after the DC component was cut. Differential IQ: Connects to tuner I (+) output after the

IC Block Diagram

TOSHIBA CONFIDENTIAL

TC90517FG Toshiba products specification [Tentative]

					DC component was cut.
31	AD_DVSS	-	-	ADC digital GND	Connects to DGND.
32	AD_DVDD	-	-	ADC digital power supply	Connects to digital +2.5 V typ.
33	VSS	-	-	Digital GND	Connects to DGND.
34	DR1VDD	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
35	VDDS	-	-	I/O power supply	Connects to digital +3.3 V typ.
36	VDDC	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
37	VSS	-	-	Digital GND	Connects to DGND.
38	STSFLG1	0	PD	Status flag 1 output	Open, fixed to L when not used.
39	DTCLK	I	PD	Pin for pre-shipment test	Open or connects to DGND.
40	DTMB	I	PU	Pin for pre-shipment test	Open or connects to digital +3.3 V typ.
41	TSMD1	I	-	Pin for pre-shipment test	Connects to DGND.
42	SYRSTN	I/O	OD	System reset input	Input at specified timing at power ON.
43	DR2VDD	-	-	Digital +2.5 V power supply	Connects to digital +2.5 V typ.
44	VSS	-	-	Digital GND	Connects to DGND.
45	SCL	I/O	OD	I2C clock input for host CPU	Connects to I2C clock bus. (Pull-up performed outside IC.)
46	SDA	I/O	OD	I2C data I/O for host CPU	Connects to I2C data bus. (Pull-up performed outside IC.)
47	VSS	-	-	Digital GND	Connects to DGND.
48	DR1VDD	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
49	VDDS	-	-	I/O power supply	Connects to digital +3.3 V typ.
50	VSS	-	-	Digital GND	Connects to DGND.
51	STSFLG0	I/O	PD	Status flag 0 output	Open, fixed to L when not used.
52	SLOCK	0		Synchronization completion (sequence 8 or higher) flag	Open, fixed to L when not used.
53	RERR	O	-	RS decoding error flag output	Open, fixed to L when not used.
54	RLOCK	O	-	RS decoding error free flag output	Open, fixed to L when not used.
55	RSEORF	O	-	TS error flag output	Open, fixed to L when not used.
56	VDDC	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
57	VSS	-	-	Digital GND	Connects to DGND.
58	PBVAL	O	-	TS valid flag output	Open, fixed to L when not used.
59	SBYTE	O	-	TS synchronization byte flag output	Open, fixed to L when not used.
60	SRDT	O	-	Serial TS data output	-
61	SRCK	O	-	TS serial clock output	-
62	VSS	-	-	Digital GND	Connects to DGND.
63	VDDC	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
64	VDDS	-	-	I/O power supply	Connects to digital +3.3 V typ.

Note 2 AGND is the abbreviation for analog GND, and DGND is the abbreviation for digital GND.

Note 3 The test dedicated pin is used for the pre-shipment test only. Make sure that processing is performed as indicated in the "Remarks" column. Any other method will lead to malfunction or failure.

Note 4 I/O indicates the type of the cell used. It may be different from the pin function because a test is conducted concurrently.

Note 5 PU indicates an I/O with a pull-up resistor (50 k Ω typ.) and PD indicates an I/O with a pull-down resistor (50 k Ω typ.). Pulling down the PU pin or pulling up the PD pin outside the IC sometimes changes the electric potential to the midpoint, resulting in instability. Caution is required.

Note 6 The unused output pins must be open and fixed to L by setting the output enable control register of each pin for noise reduction or to the output OFF state.

Note 7 OD indicates an open drain I/O. To use the pin for output, pull up the resistance outside the IC.

* The following pins are added with the upgrade from TC90507 to TC90517 (except the changes of power supply and GND pins):

Pin Number	Pin Name	Description
21	FIL	Added to the PLL loop filter.
27	ADQ_AIN	Added for IQ input (differential).
28	ADQ_AIP	Added for IQ input.
7	AGCI	Added to passthrough the AGC control signal of other ICs.
52	SLOCK	Changed from conventional FLOCK.

PRELIMINARY W9751G6JB



4. BALL CONFIGURATION

1	2	3	4	5	6	7	8	9
VDD	NC	VSS		A		VSSQ	\overline{UDQS}	VDDQ
DQ 14	VSSQ	UDM		B		UDQS	VSSQ	DQ 15
VDDQ	DQ 9	VDDQ		C		VDDQ	DQ 8	VDDQ
DQ 12	VSSQ	DQ 11		D		DQ 10	VSSQ	DQ 13
VDD	NC	VSS		E		VSSQ	\overline{LDQS}	VDDQ
DQ 6	VSSQ	LDM		F		LDQS	VSSQ	DQ 7
VDDQ	DQ 1	VDDQ		G		VDDQ	DQ 0	VDDQ
DQ 4	VSSQ	DQ 3		H		DQ 2	VSSQ	DQ 5
VDDL	VREF	VSS		J		VSSDL	CLK	VDD
	CKE	\overline{WE}		K		\overline{RAS}	\overline{CLK}	ODT
NC	BA0	BA1		L		\overline{CAS}	\overline{CS}	
	A10/AP	A1		M		A2	A0	VDD
VSS	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	VSS
VDD	A12	NC		R		NC	NC	

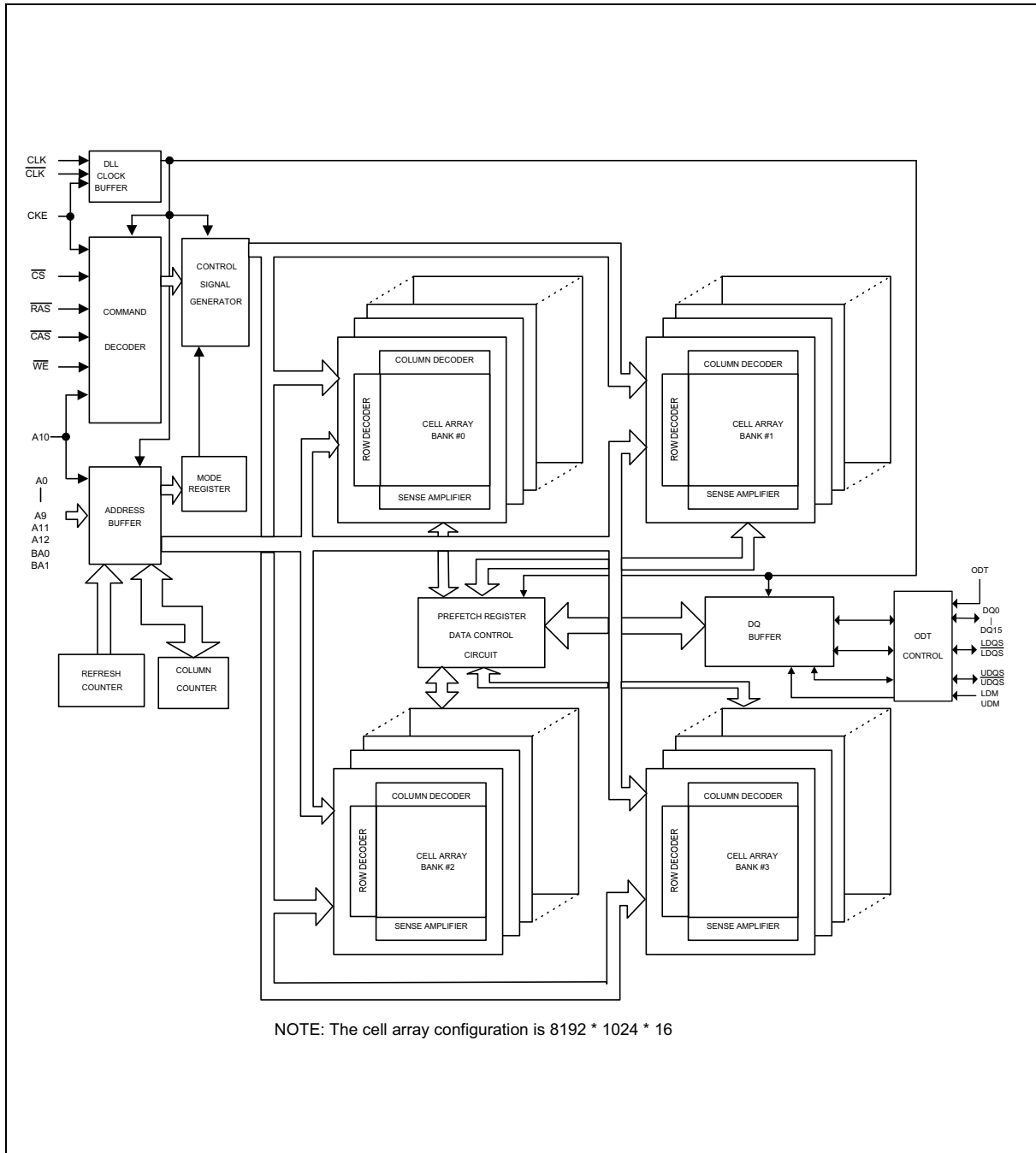


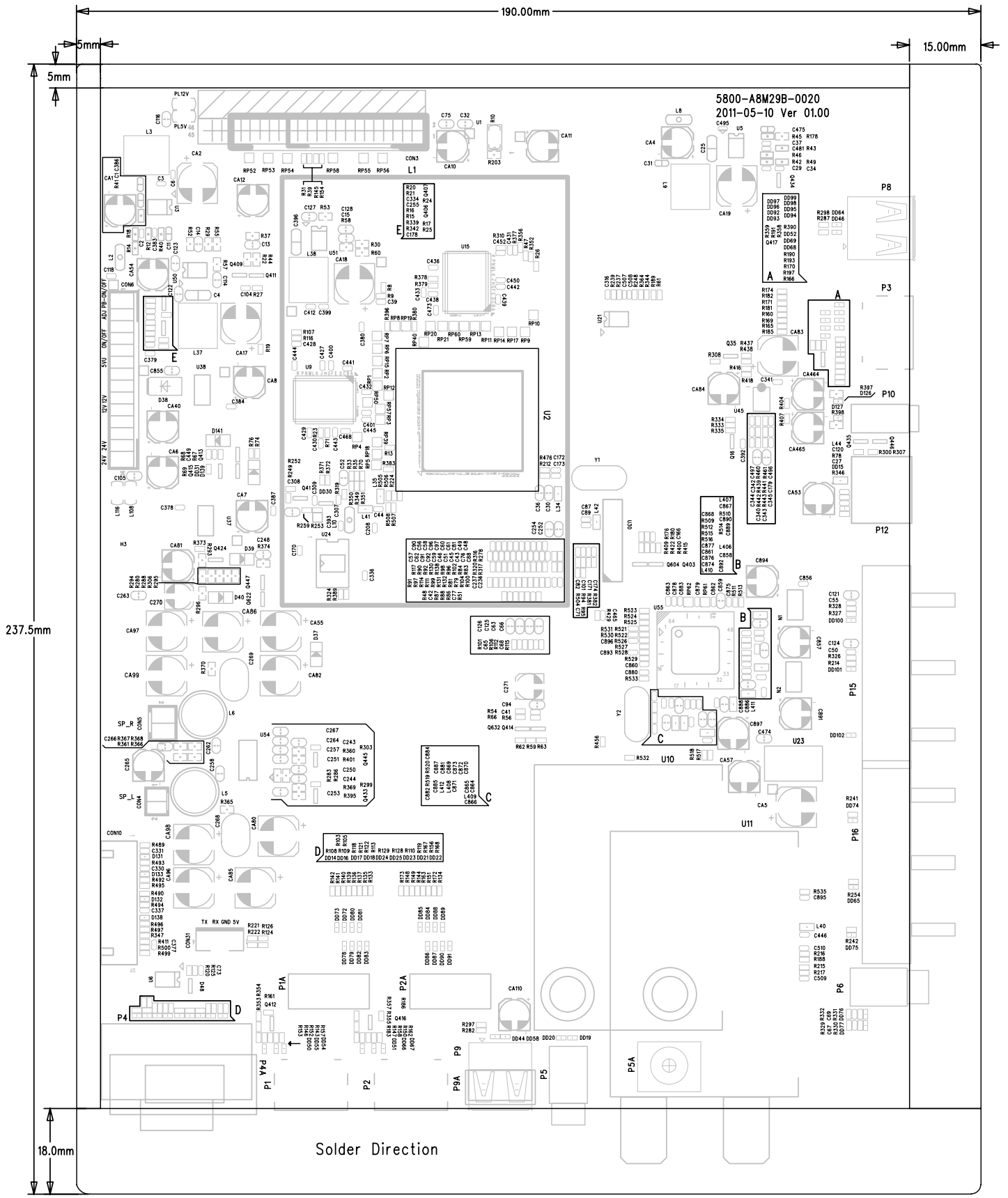
5. BALL DESCRIPTION

BALL NUMBER	SYMBOL	FUNCTION	DESCRIPTION
M8,M3,M7,N2,N8,N3,N7,P2,P8,P3,M2,P7,R2	A0–A12	Address	Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. Row address: A0–A12. Column address: A0–A9. (A10 is used for Auto-precharge)
L2,L3	BA0–BA1	Bank Select	BA0–BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
G8,G2,H7,H3,H1,H9,F1,F9,C8,C2,D7,D3,D1,D9,B1,B9	DQ0–DQ15	Data Input / Output	Bi-directional data bus.
K9	ODT	On Die Termination Control	ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM.
F7,E8	LDQS, $\overline{\text{LDQS}}$	LOW Data Strobe	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS corresponds to the data on DQ0–DQ7. $\overline{\text{LDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
B7,A8	UDQS, $\overline{\text{UDQS}}$	UP Data Strobe	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS corresponds to the data on DQ8–DQ15. $\overline{\text{UDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
L8	$\overline{\text{CS}}$	Chip Select	All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple ranks. $\overline{\text{CS}}$ is considered part of the command code.
K7,L7,K3	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$	Command Inputs	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{CS}}$ (along with $\overline{\text{CS}}$) define the command being entered.
B3,F3	UDM LDM	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
J8,K8	CLK, $\overline{\text{CLK}}$	Differential Clock Inputs	CLK and $\overline{\text{CLK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{\text{CLK}}$. Output (read) data is referenced to the crossings of CLK and $\overline{\text{CLK}}$ (both directions of crossing).
K2	CKE	Clock Enable	CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
J2	VREF	Reference Voltage	VREF is reference voltage for inputs.
A1,E1,J9,M9,R1	VDD	Power Supply	Power Supply: 1.8V ± 0.1V.
A3,E3,J3,N1,P9	VSS	Ground	Ground.
A9,C1,C3,C7,C9,E9,G1,G3,G7,G9	VDDQ	DQ Power Supply	DQ Power Supply: 1.8V ± 0.1V.
A7,B2,B8,D2,D8,E7,F2,F8,H2,H8	VSSQ	DQ Ground	DQ Ground. Isolated on the device for improved noise immunity.
A2,E2,L1,R3,R7,R8	NC	No Connection	No connection.
J7	VSSDL	DLL Ground	DLL Ground.
J1	VDDL	DLL Power Supply	DLL Power Supply: 1.8V ± 0.1V.

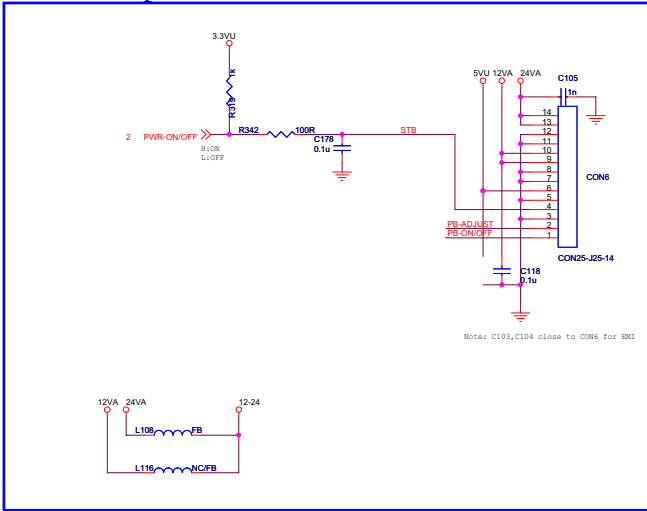


6. BLOCK DIAGRAM

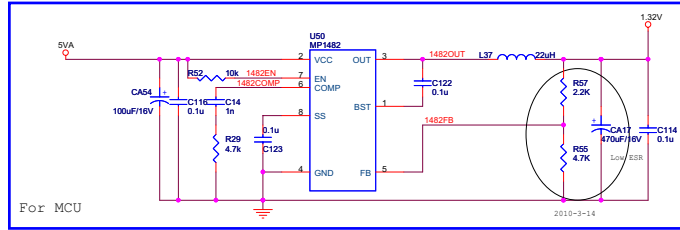




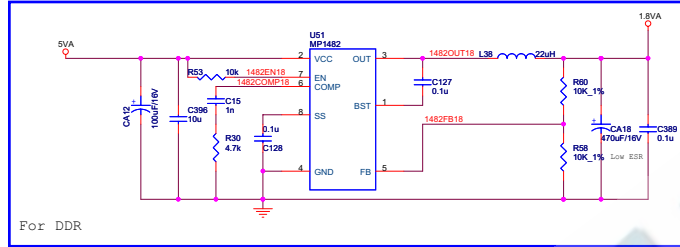
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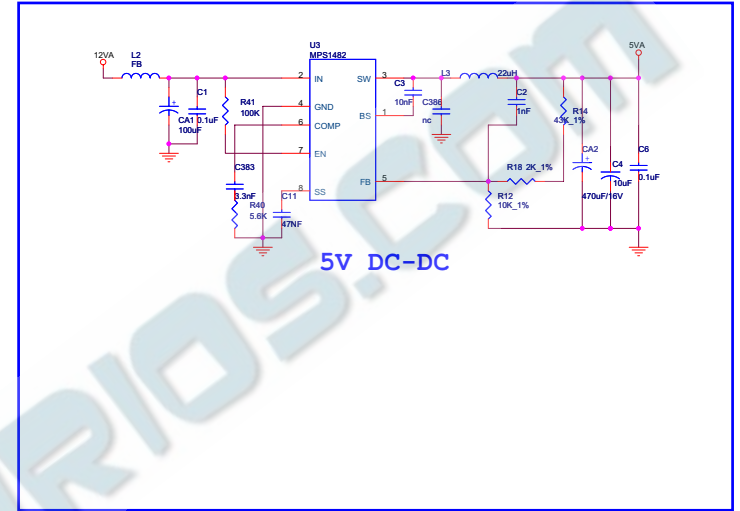
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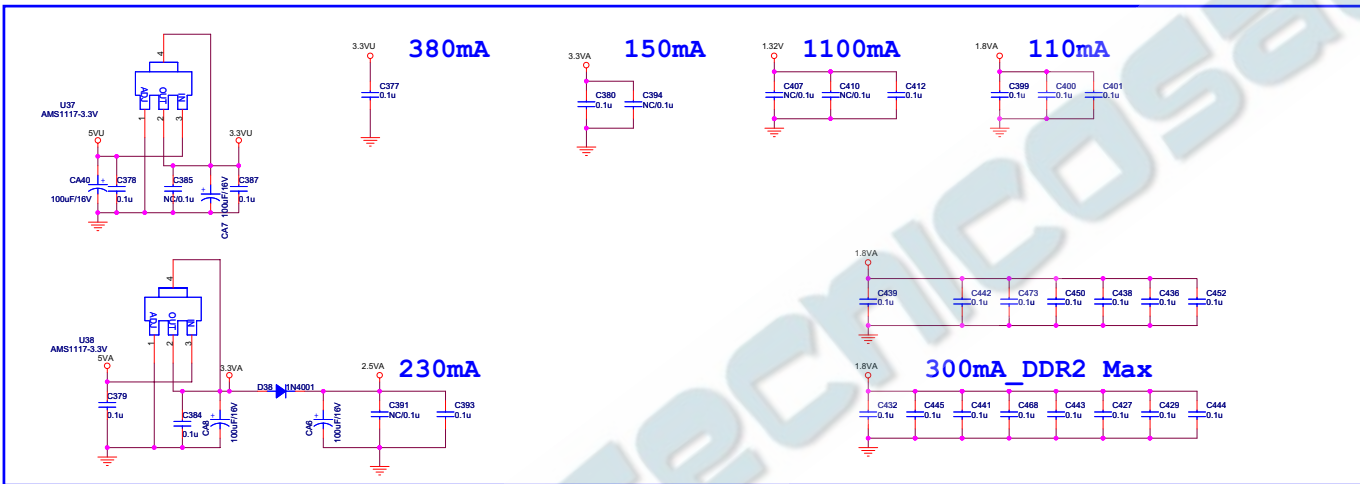
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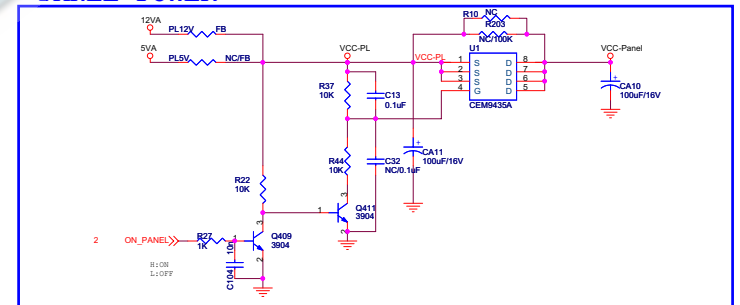
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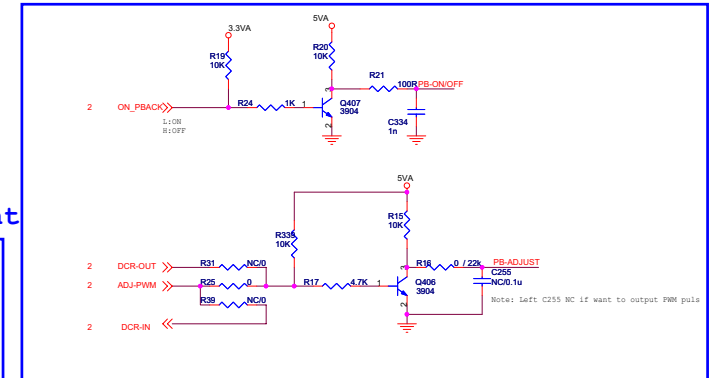
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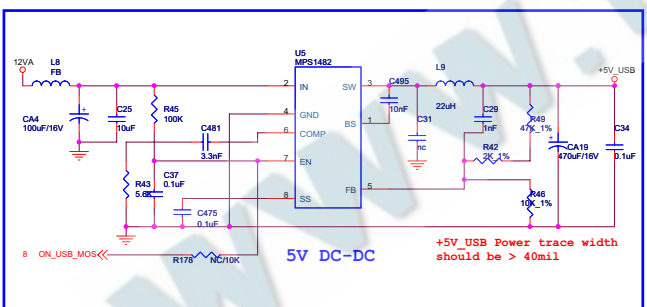
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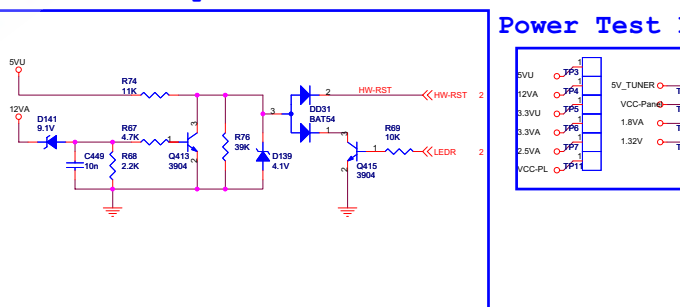
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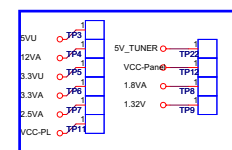
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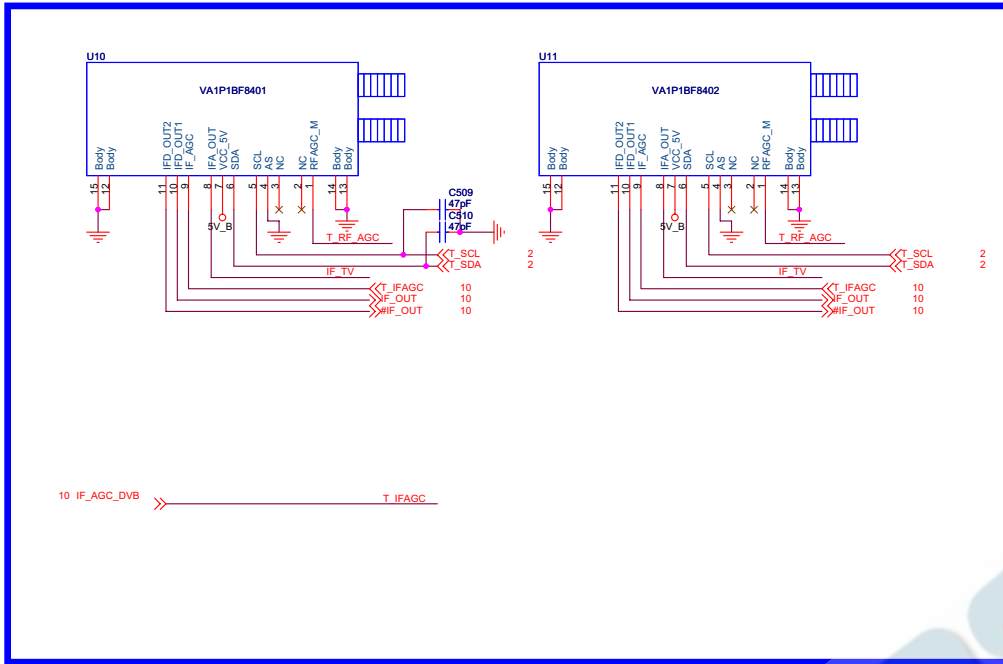
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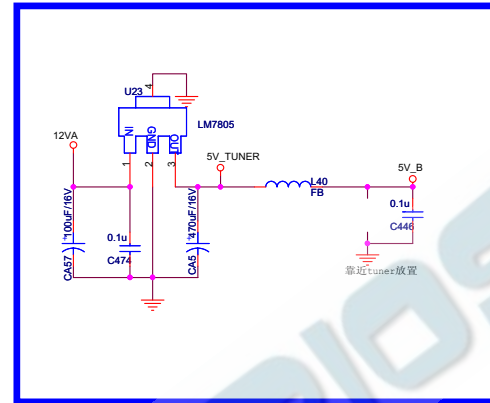
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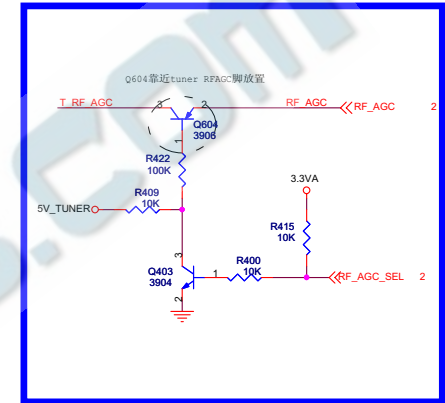
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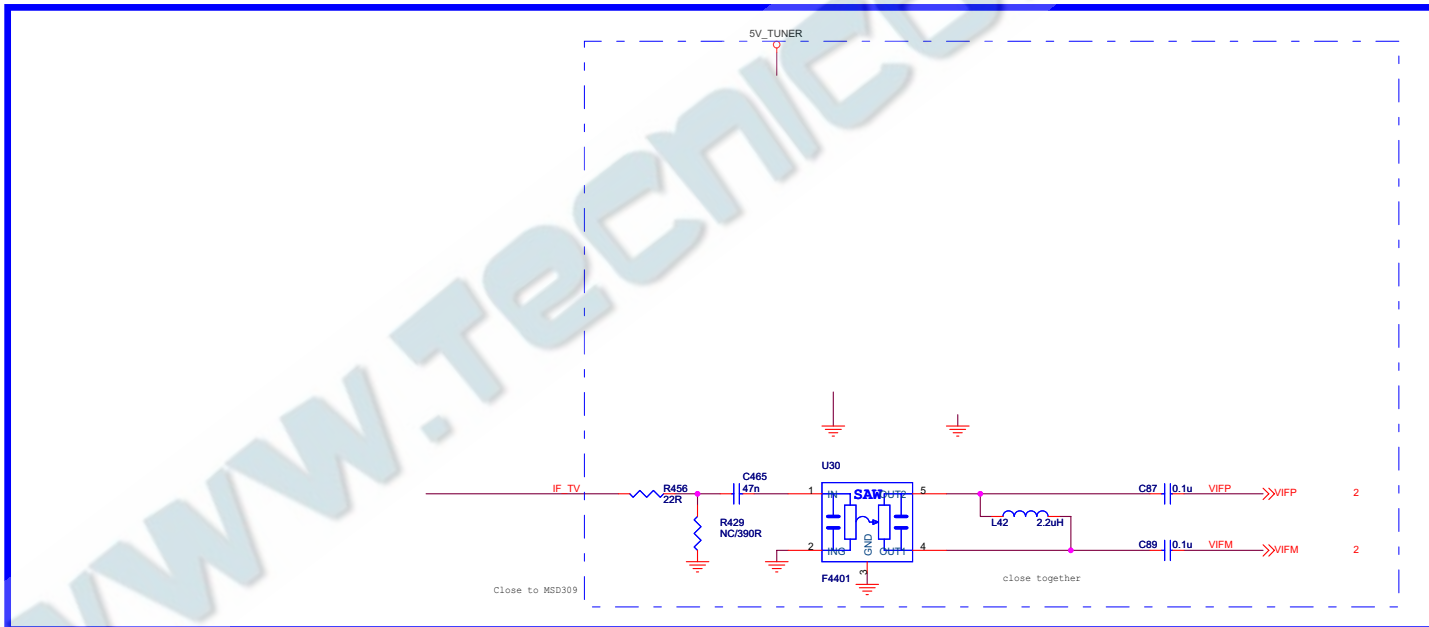
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RF AGC Switch

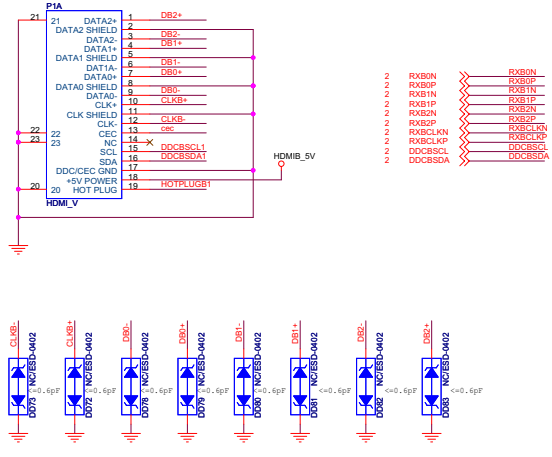
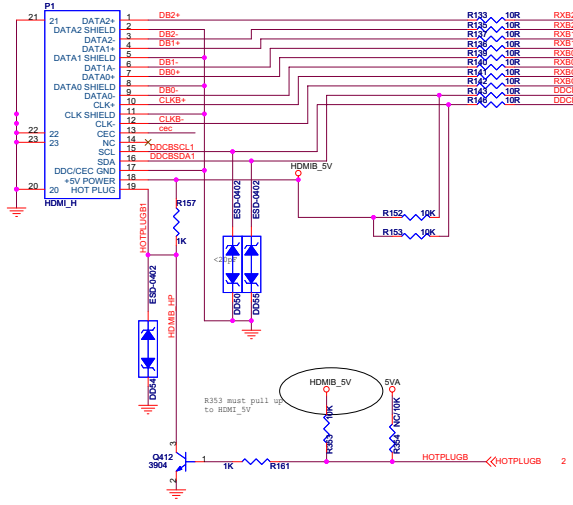


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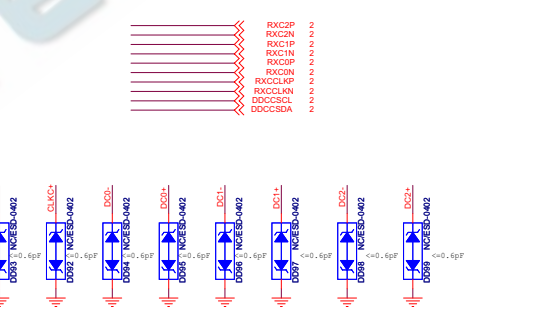
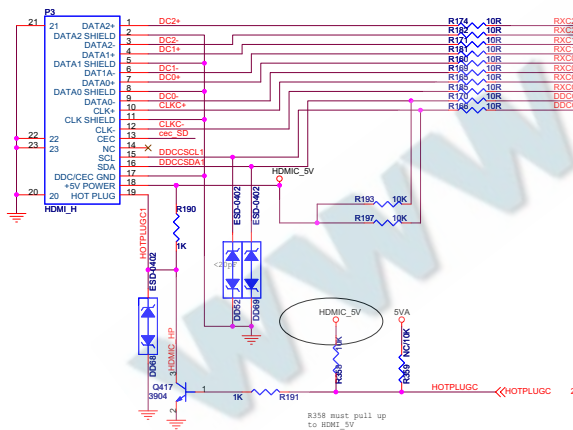
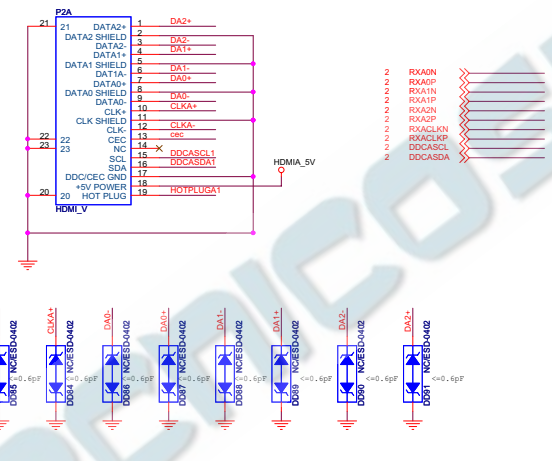
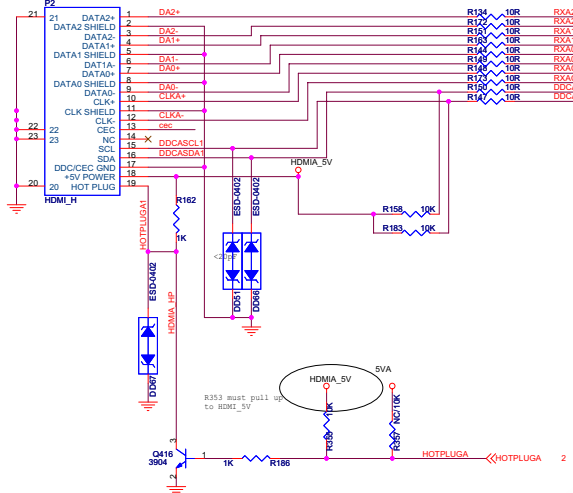
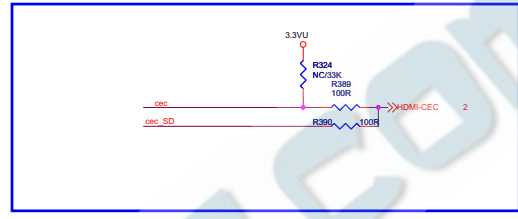


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HDMI Input

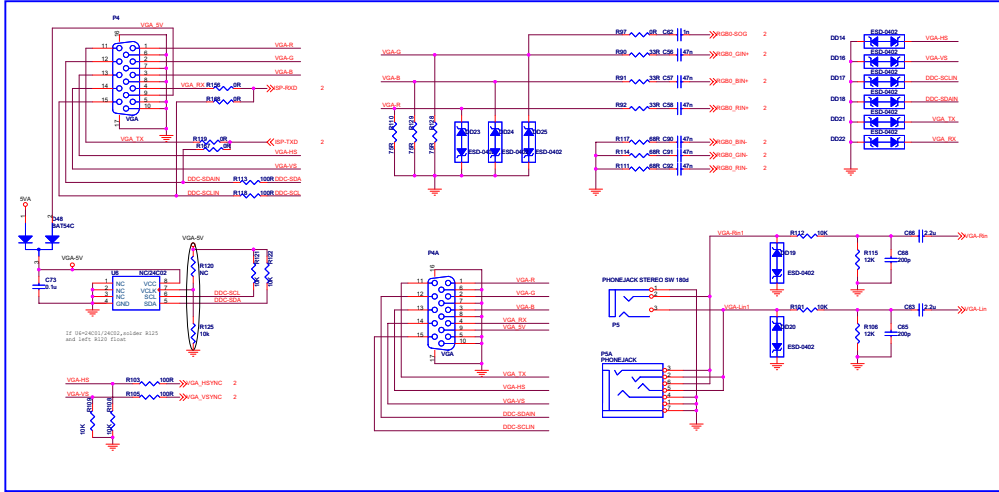


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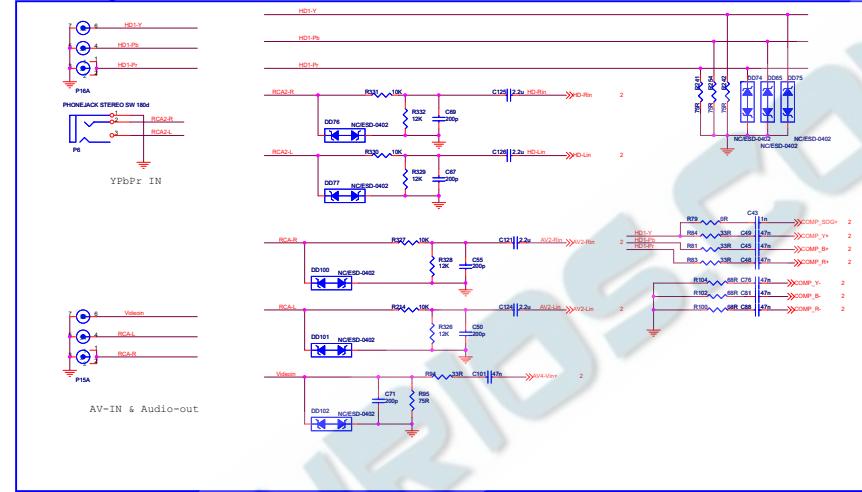


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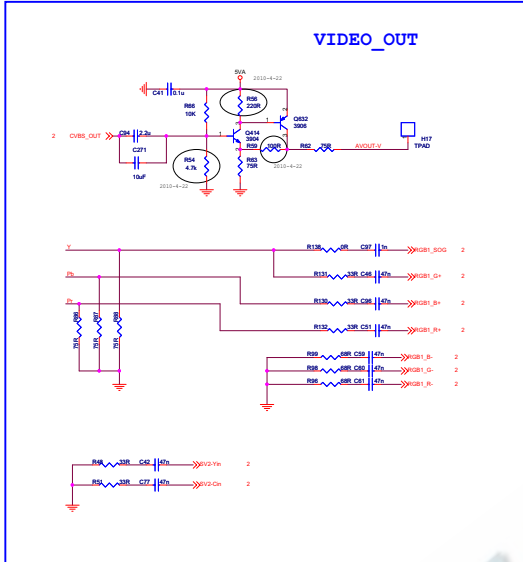
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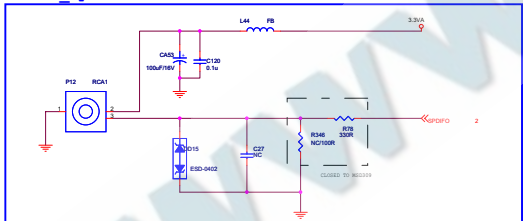
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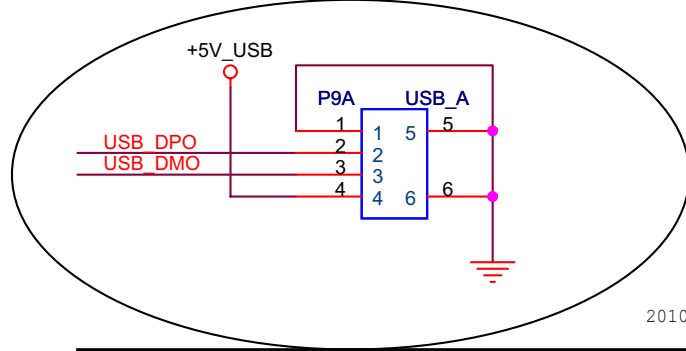
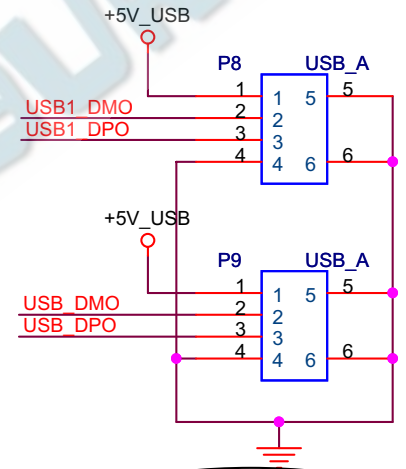
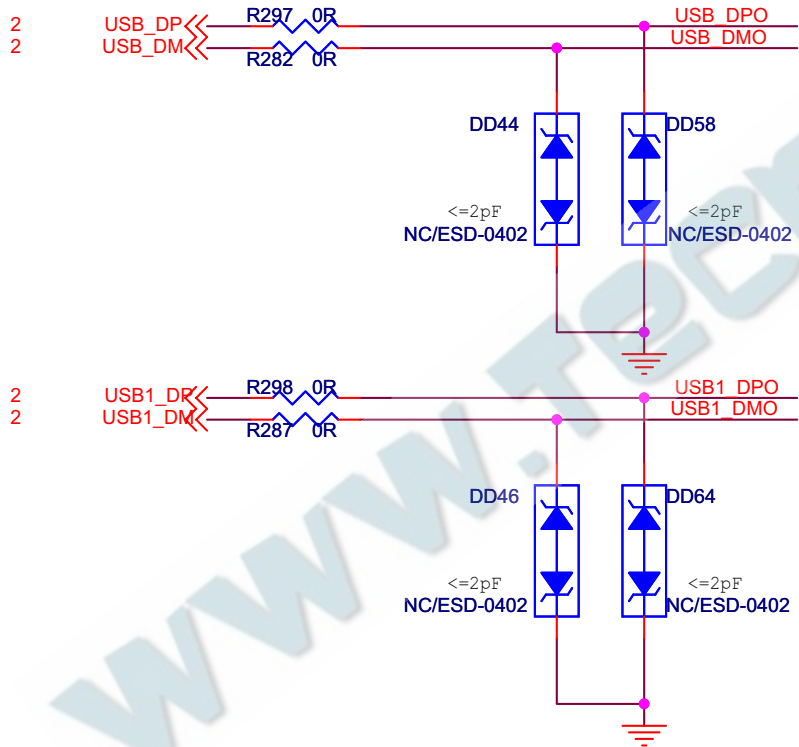
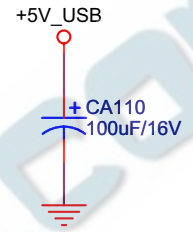
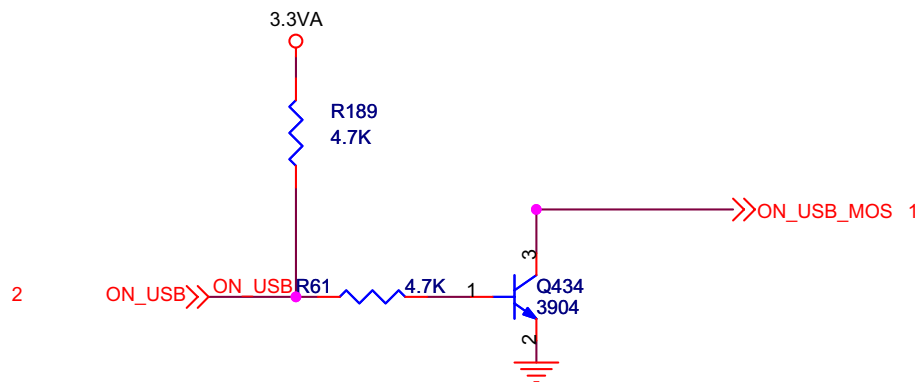


FOR UN-USED PORTS



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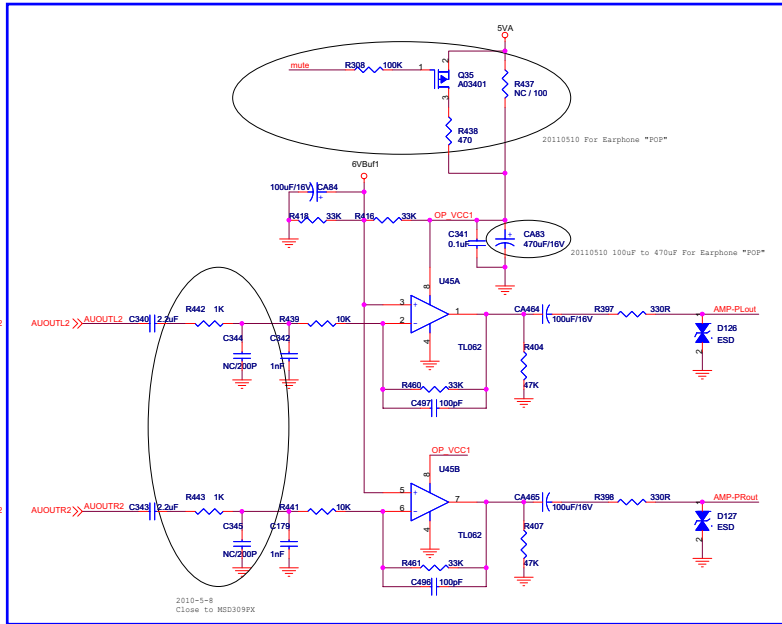




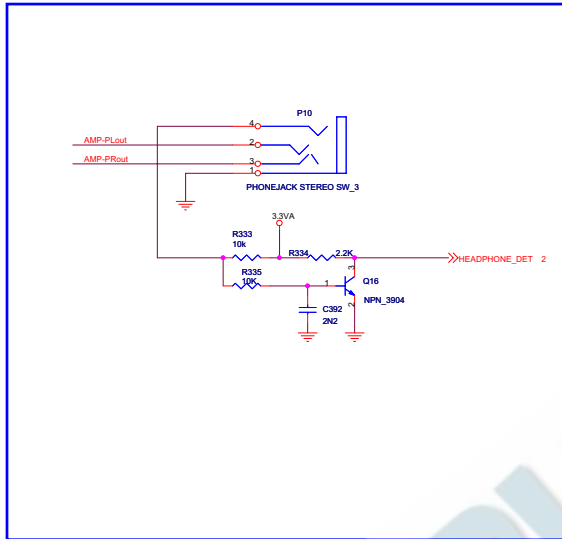
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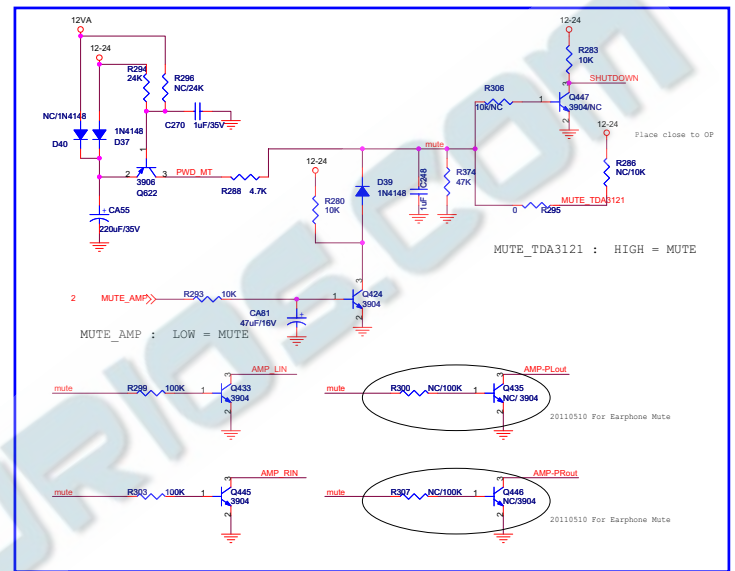
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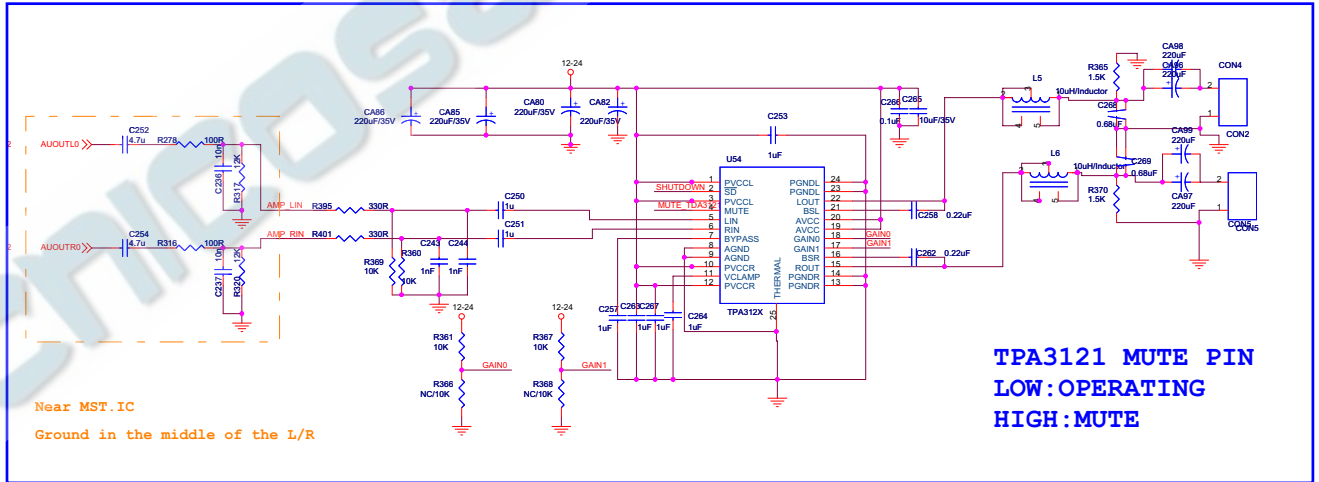
HeadPhone Out



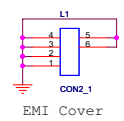
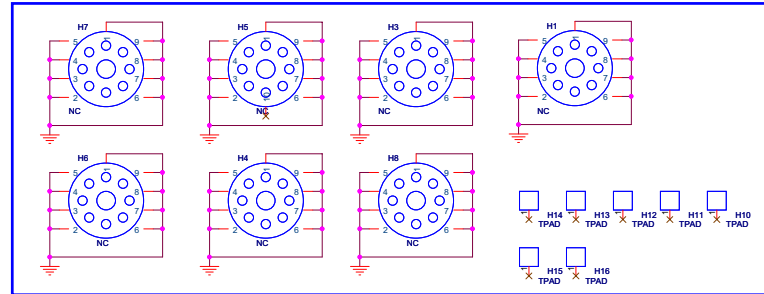
Power Down MUTE

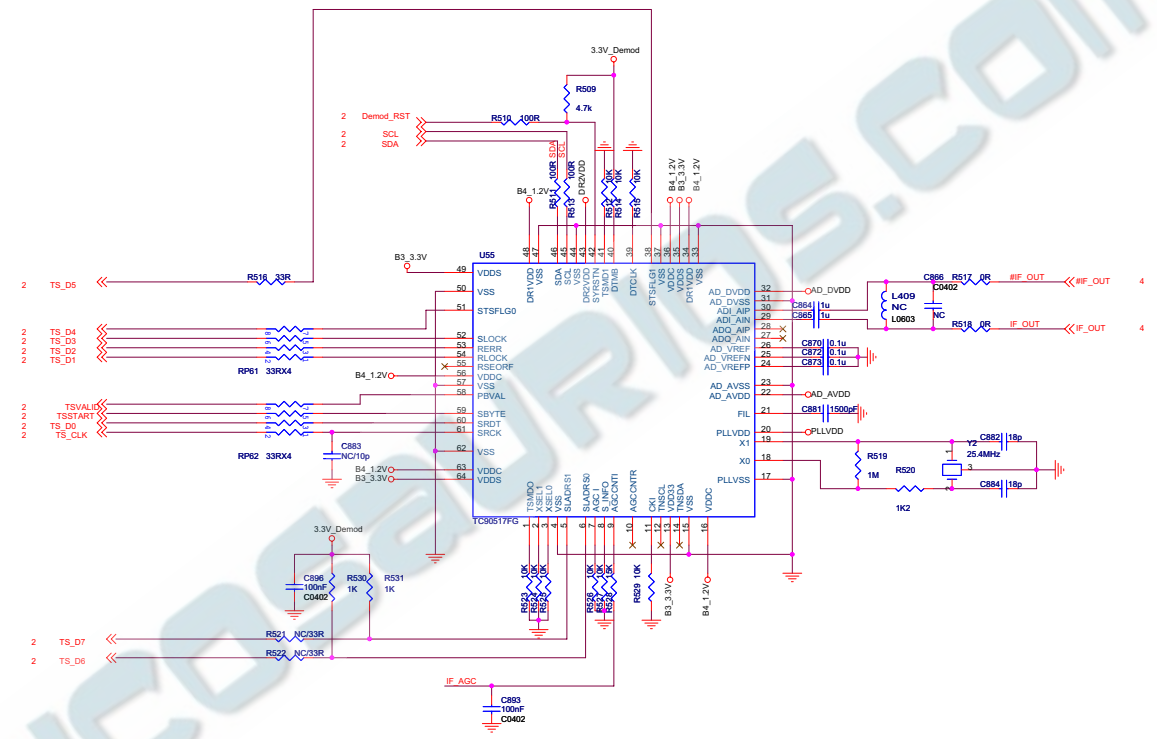
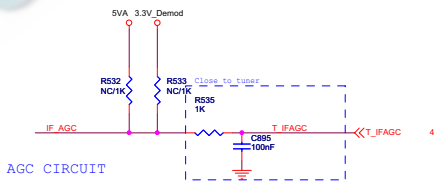
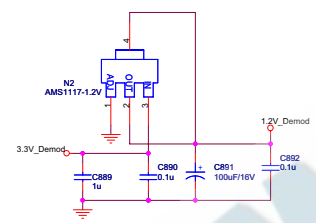
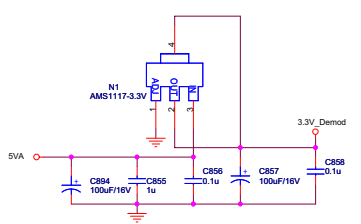
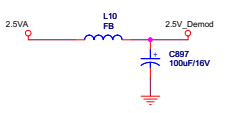
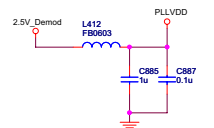
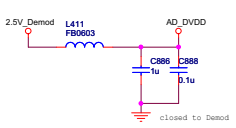
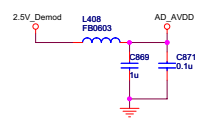
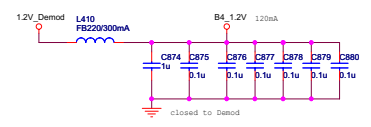
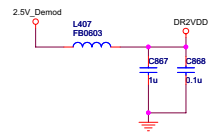
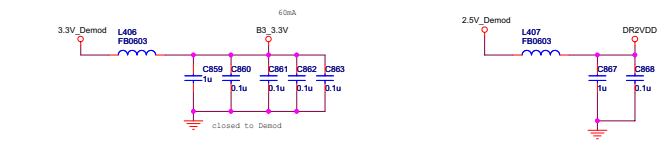


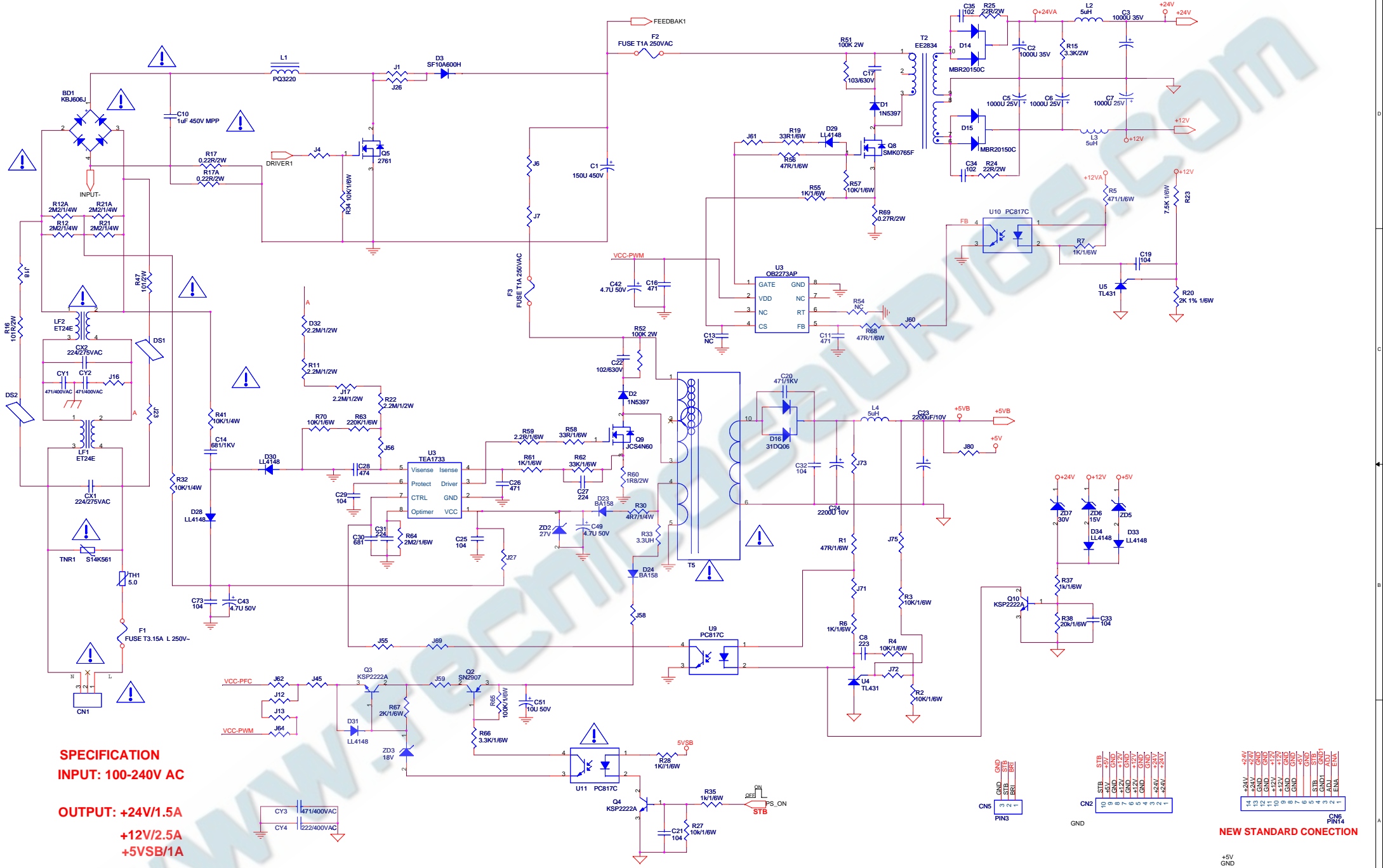
TDA3121



HOLE



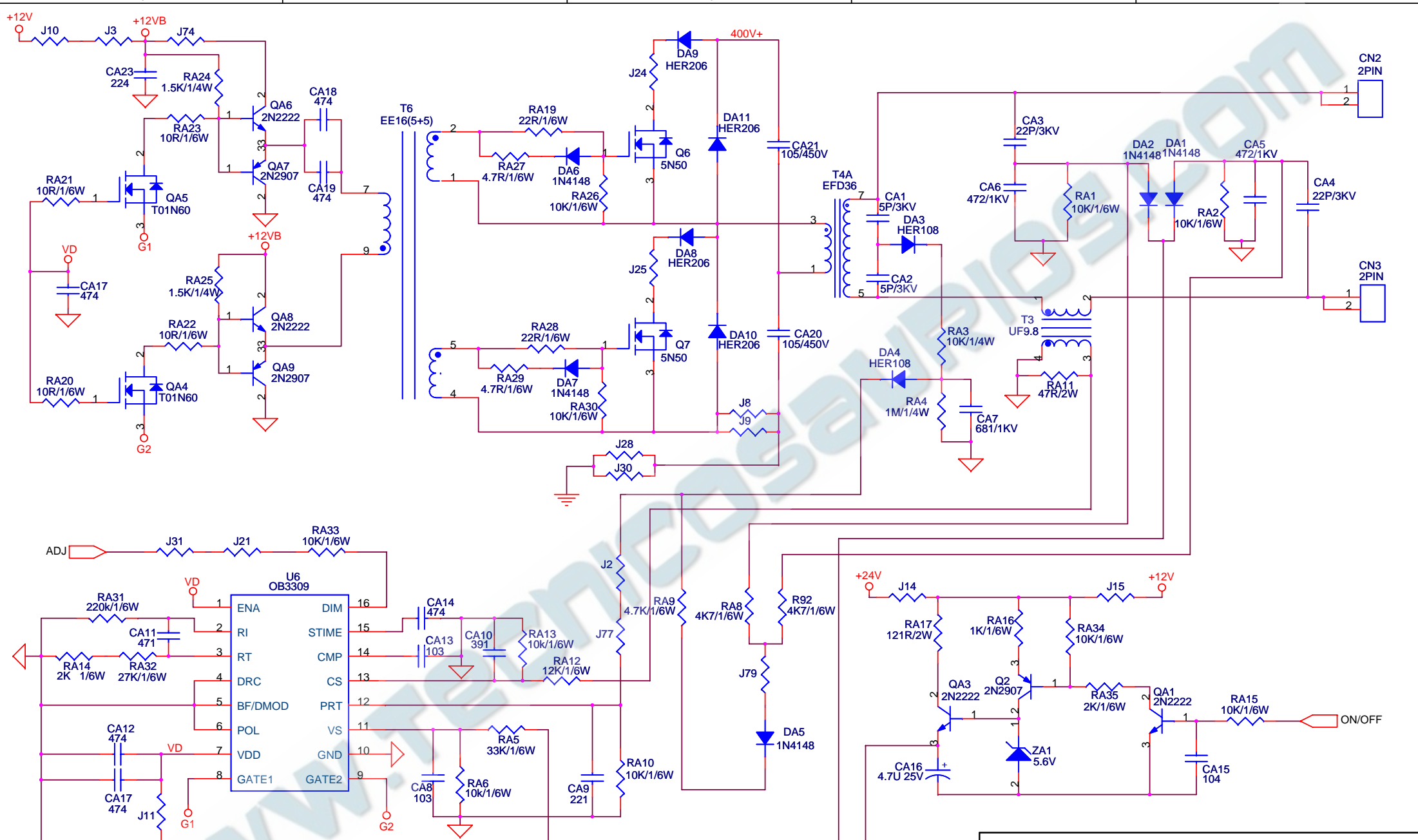




SPECIFICATION
INPUT: 100-240V AC
OUTPUT: +24V/1.5A
+12V/2.5A
+5VSB/1A
OUTPUT: +12V/4.5A



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